DIGI-DATA CORPORATION
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DIGI-DATA
MICROPROCESSOR-CONTROLLED
FORMATTER
OPERATION MANUAL

0552700-0000

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RECORD OF REVISIONS

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1 - GENERAL DESCRIPTION

1.1 INTRODUCTION. This manual describes the specifications, interfacing, operation and maintenance of the microprocessor controlled embedded formatter manufactured by Digi-Data Corporation, Jessup, Maryland. This section includes the formatter's functional capabilities, physical characteristics, and specifications. The formatter is available in three configurations, all of which mount on the transport.

1) NRZ only
2) PE only
3) NRZ/PE

1.2 PURPOSE OF EQUIPMENT. The Digi-Data Formatter is designed for use exclusively with the 1840, 1740, 1640 and 1140 series synchronous transports manufactured by Digi-Data Corporation. The formatter handles any mix of seven track and nine track, NRZ, PE and dual density transports with tape speeds from 12.5 to 75 IPS. Magnetic tapes generated by any -40 series transport equipped with a formatter are fully compatible with ANSI and IBM specifications.

1.3 PHYSICAL DESCRIPTION. The formatter is a 7 5/8" x 16 3/4" (19.3 cm x 42.6 cm) printed circuit card assembly. In the NRZ/PE and PE only configurations, the card assembly contains 150 integrated circuit packages; the NRZ only configuration contains 88 ICs. The microprocessor consists of a pair of bipolar bit slice units. The NRZ/PE program, containing approximately 800 32-bit microinstructions, is stored in four 1024 x 8 bi-polar PROMs; the NRZ or PE only microprograms are stored in four 512 x 8 PROMs. PROMs are also employed for several decoding and control functions.

The formatter may be mounted on any -40 series transport. All input-output connections are made via 50 conductor ribbon cable plug connectors. The power connection (+5VDC and GND) is made via a separate cable from the host transport.

1.4 FUNCTIONAL DESCRIPTION. Motion control conforms entirely to ANSI standards. The formatter supports six tape speeds, decoding the three speed status lines from the -40 series transport as follows:

SP 0	SP 1	SP 2	Tape Speed
LO	HI	HI	12.5 IPS
HI	LO	HI	18.75 IPS
LO	LO	HI	25 IPS
HI	HI	LO	37.5 IPS
LO	HI	LO	45 IPS
HI	LO	LO	75 IPS

The required extended gaps are inserted from BOT and preceding file marks.

Data format also conforms to ANSI specifications. The data format status lines from the -40 series transport decode as follows:

FMT1	FMT2	FMT3	Format
LO	LO	LO	7 track, 200 BPI, NRZ
LO	LO	HI	7 track, 556 BPI, NRZ
HI	LO	LO	7 track, 800 BPI, NRZ
LO	HI	LO	9 track, 200 BPI, NRZ (see paragraph 3.5)
HI	HI	LO	9 track, 800 BPI, NRZ
LO	HI	HI	9 track, 1600 BPI, PE

In PE, the formatter generates and detects the preamble, postamble, ID burst, and file marks. When reading, data is recovered, decoded, deskewed, and buffered; single channel drop-outs are also detected and corrected.

In NRZ, the formatter generates the Cyclic Redundancy Check Character (CRCC; 9 track 800 BPI only), odd or even vertical parity, and end-of-file marks. During read and read-after-write (dual gap) operations, the CRCC is regenerated and checked bit-for-bit (9 track 800 BPI only), the LRCC and vertical parity are verified, and file marks are detected.

The formatter controls sixteen different tape operations. Write and erase operations may be performed only in the forward direction; reading may be performed in either direction. Previously recorded tapes may be edited. The controller command signals are decoded as illustrated in Figure 3-1. Each operation is fully described in paragraph 3.2.

Three types of operations are illegal and result in a special formatter sequence. The illegal operations are 1) issuing a write or erase command in the reverse direction, 2) any reverse operation at BOT, and 3) NRZ selected on a PE formatter or PE selected on a NRZ formatter. The formatter cycles the FBY and DBY lines as though an operation equal in duration to the normal ramp up/ramp down time has occurred and then sets both the HER and CER flags. The tape is not moved. If BOT is encountered while performing a legal reverse operation the formatter is cleared and the tape is stopped. The HER and CER flags are set and tape motion is halted if 25 feet of tape are read without encountering data or if no read data occurs while writing with a dual gap head.

The formatter may be mounted on any -40 series transport. A transport containing a formatter is designated a "master transport". Up to three additional transports may be daisy-chained to the master transport. These additional transports do not contain formatters and are consequently designated "slave transports". The slave transports may differ from the master transport and from each other in tape speed, head type, number of tracks, data packing density, recording mode, and reel size; there are no restrictions upon variety in a system.

1.5 PLUG JUMPER OPTIONS.

1.5.1 LAST WORD FORMAT.

With the plug jumper in position WS LWD is signalled coincident with the last data character to be written; this is the normal usage. With the plug jumper in position WR LWD is signalled after the last required WSTR but before another occurs.

1.5.2 CHECK CHARACTERS. With the plug jumper in position WN NRZ check character(s) are passed to the controller. With the jumper in WP the check character(s) are truncated in the formatter. The latter is the normal usage.

1.5.3 GATE EXTERNAL PARITY. External parity may be generated by two methods:

1) With the jumper in position WB the controller may generate and gate external parity into the formatter by holding the I/O signal GATE WP true. This is the more common method.

2) With the jumper in position WA, GATE WP is forced low and the controller must generate external parity for the formatter.

Internal parity may be generated by installing the jumper in position WB and holding the I/O signal GATE WP false. Installing the jumper in position WB thus permits either internal or external parity to be generated simply by toggling GATE WP. Jumper position WA only permits external parity.

1.5.4 FORMATTER ADDRESS. These three plug jumper positions permit the formatter to respond to either FAD Ø (WH), FAD 1 (WK), or both (WJ).

1.5.5 DENSITY SELECT. The DDS line to the transport follows the controller signal DEN with the plug jumper in position WE. This is the normal usage. With the jumper in position WF the DDS line follows the controller signal FAD. In this situation the controller may properly select either density of a 9 track 800/1600 BPI transport without manipulating the DEN line. (PE is then FADØ and NRZ FAD1.)

1.5.6 FORMATTER CLEAR. The formatter is cleared by power-up with jumper WL installed. When WM is installed the formatter is cleared when RDY goes false in the selected transport.

1.6 SPECIFICATIONS

Characteristic	Value
Recording Mode	PE and NRZ.
Number of Channels	7 and 9
Data Density	200, 556, 800, and 1600 BPI.
Tape Speeds	12.5, 18.75, 25, 37.5, 45, 75 IPS.
Electrical Interface	TTL, open collector, low true.
Physical Configuration	Printed circuit card assembly, 7-5/8" x 16-3/4", mounted on transport.

Weight	2.0 pounds max.
Operating Environment	To 20,000 feet (6,000 m.), 32 to 122°F (0 to 50°C), to 95% RH W/O condensation.
Storage Environment	To 50,000 feet (15,00 m.), -40 to 158°F (-40 to 70°C).
Cooling	Convection. Forced air may be required in confined areas.
Options	Controller I/O pin-outs: Digi-Data or industry standard alternate.
	Last Word: Synchronous or Asynchronous.
	Formatter Address: 0, 1, or both.
	External Parity: Yes, no, or via GATE WP signal.
	Density Select: Via DEN signal or via FAD signal.
	Formatter Clear: Via Power up or Transport RDY.

2 - INTERFACE CONNECTION

2.1 INTRODUCTION. This section summarizes electrical and physical interface requirements.

2.2 ELECTRICAL INTERFACE. Logic levels for all I/O lines are low true.

ONE = LOW = TRUE = 0 to 0.6 VDC
ZERO = HIGH = FALSE = greater than 2.0 VDC

Minimum input pulse width on all lines is 500 nanoseconds. The command lines (WRT, ERASE, REV, RTH1, RTH2, EDIT, WFM, DEN, PAR) must be established 100 nanoseconds before the trailing edge of GO. All lines are terminated in a 220-ohm resistor to V_{CC} and a 330-ohm resistor to ground. No more than one receiver load exists on any input line. Outputs are driven by 7406/7407 open collector hex drivers or the equivalent, capable of sinking 40 mA. The recommended interface circuit is shown in figure 2-1.

2.3 POWER SPECIFICATIONS. The formatter draws a maximum of 7.5A from the host transport's +5 VDC supply in the NRZ/PE and PE only configurations, and a maximum of 4.5A in the NRZ only configuration. The host transport's +5 VDC supply should be adjusted to 5.0 ± 0.25V. Short circuit and overvoltage protection is provided in the host transport.

2.4 PHYSICAL INTERFACE. Two fifty conductor ribbon cables are required for the controller I/O. The cables should plug into either the Digi-Data interface concectors JA and JB, or into the alternate interface connectors JC and JD. Figures 2-2, 2-3, and 2-4 list the pinouts for both. Maximum cable length is 20 feet.

2.5 DAISY-CHAIN CONNECTIONS. Ribbon cables are available for connecting one, two, or three slave transports to the formatted master transport. Refer to figure 2-5 for part numbers.

Two formatters may be daisy-chained so that eight transports may be addressed from a single controller. When formatters are daisy-chained the three termination packs mounted in sockets must be removed from the first formatter in the chain. See figure 2-6.

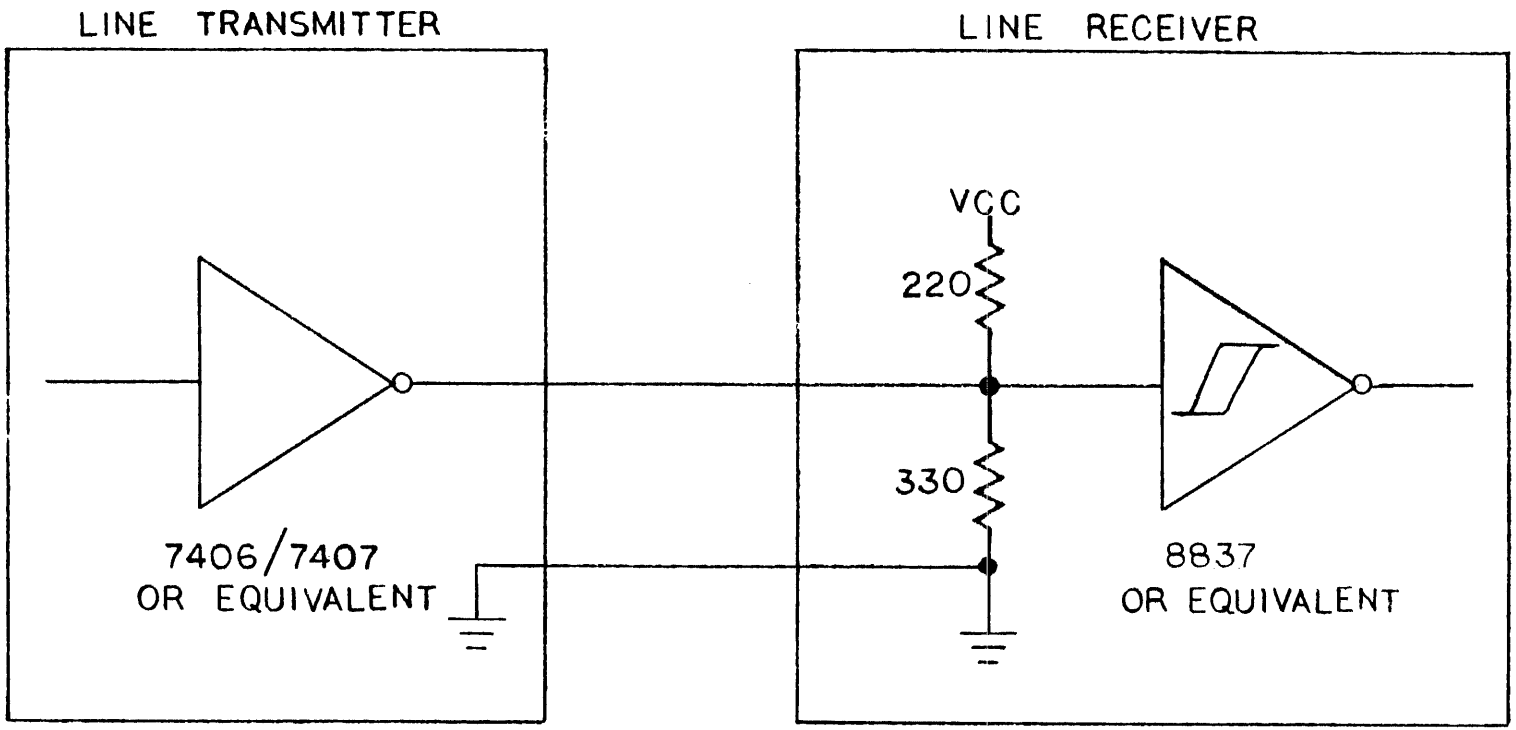


FIGURE 2-1, RECOMMENDED INTERFACE CIRCUIT

JA

1	(+5V)	GND	2
3	WP.C	GND	4
5	W0	GND	6
7	W1	GND	8
9	W2.B	GND	10
11	W3.A	GND	12
13	W4.8	GND	14
15	W5.4	GND	16
17	W6.2	GND	18
19	W7.1	GATEWP	20
21	FBY	GND	22
23	DBY	INDENT/CCG	24
25	DEN STAT	GND	26
27	HER	CER	28
29	FMK	GND	30
31	CCG	7 TK	32
33	RDY	GND	34
35	ONL	GND	36
37	RWD	GND	38
39	THR2	THR1	40
41	ERASE	GND	42
43	EDIT	WFM	44
45	WRITE	GND	46
47	REV	GND	48
49	OFL	GND	50

JB

1	REW	GND	2
3	TAD1	GND	4
5	TAD0	GND	6
7	LWD	GND	8
9	FPT	GND	10
11	LPT	GND	12
13	EOT	GND	14
15	NRZ	LOL	16
17	SGL	GND	18
19	SPD SEL	GND	20
21	WSTR	GND	22
23	RSTR	GND	24
25	R0	GND	26
27	R1	GND	28
29	R2.B	GND	30
31	R3.A	GND	32
33	R4.8	GND	34
35	R5.4	GND	36
37	R6.2	GND	38
39	R7.1	GND	40
41	RP.C	GND	42
43	FEN	GND	44
45	FAD	GND	46
47	GO	GND	48
49	PAR	DEN	50

Figure 2-2, Controller I/O (Digi-Data)

JC

1	GND	FBY	2
3	GND	LWD	4
5	GND	W4.8	6
7	GND	GO	8
9	GND	WO	10
11	GND	W1	12
13	GND	SGL	14
15	GND	LOL	16
17	GND	REV	18
19	GND	REW	20
21	GND	WP.C	22
23	GND	W7.1	24
25	GND	W3.A	26
27	GND	W6.2	28
29	GND	W2.B	30
31	GND	W5.4	32
33	GND	WRITE	34
35	GND	THR2	36
37	GND	EDIT	38
39	GND	ERASE	40
41	GND	WFM	42
43	GND	THR1	44
45	GND	TADO	46
47	GND	R2.B	48
49	GND	R3.A	50

JD

1	RP.C	RO	2
3	R1	LPT	4
5	GND	R4.8	6
7	GND	R7.1	8
9	GND	R6.2	10
11	GND	HER	12
13	GND	FMK	14
15	GND	CCG/IDENT	16
17	GND	FEN	18
19	GND	R5.4	20
21	GND	EOT	22
23	GND	OFL	24
25	GND	NRZ	26
27	GND	RDY	28
29	GND	RWD	30
31	GND	FPT	32
33	GND	RSTR	34
35	GND	WSTR	36
37	GND	DBY	38
39	GND	SPEED	40
41	GND	CER	42
43	GND	ONL	44
45	GND	TAD1	46
47	GND	FAD	48
49	GND	DEN	50

Figure 2-3, Controller I/O (Alternate)

USE THIS!
in JC, JD.

JE

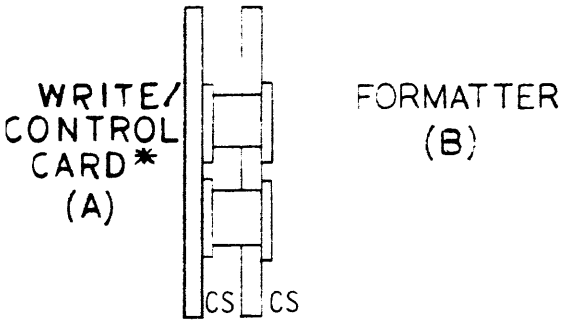
1	FMT2	SP1	2
3	SGL	GND	4
5	SP0	SP2	6
7	RDY	GND	8
9	ONL	GND	10
11	RWD	GND	12
13	FPT	GND	14
15	LDP	GND	16
17	EOT	GND	18
19	FMT3	SPS	20
21	---	GND	22
23	SWS	GND	24
25	WARS	GND	26
27	WDS	GND	28
29	RTH2	GND	30
31	RTH1	GND	32
33	OVW	GND	34
35	SLT2	GND	36
37	SLT3	GND	38
39	SLT0	GND	40
41	SLT1	GND	42
43	SFC	GND	44
45	SRC	GND	46
47	(+5V)	(GND)	48
49	(+5V)	(GND)	50

JF

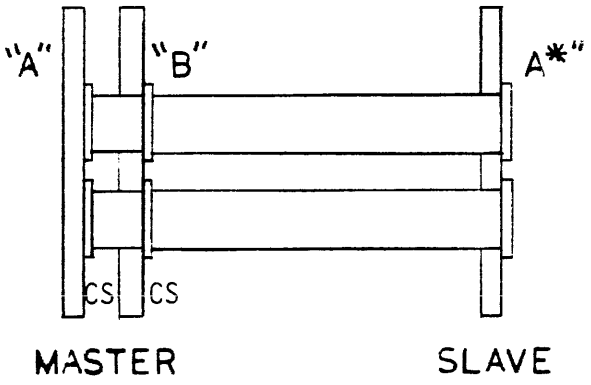
1	RWC	GND	2
3	OFFC	GND	4
5	WD7.1	GND	6
7	WD6.2	GND	8
9	WD5.4	GND	10
11	WD4.8	GND	12
13	WD3.A	GND	14
15	WD2.B	GND	16
17	WD1	GND	18
19	WD0	GND	20
21	WDP.C	GND	22
23	DDS	GND	24
25	RDS	GND	26
27	RD7.1	GND	28
29	RD6.2	GND	30
31	RD5.4	GND	32
33	RD4.8	GND	34
35	RD3.A	GND	36
37	RD2.B	GND	38
39	RD1	GND	40
41	RD0	GND	42
43	ROL	GND	44
45	(RDIS)	GND	46
47	RDP.C	GND	48
49	FMT1	GND	50

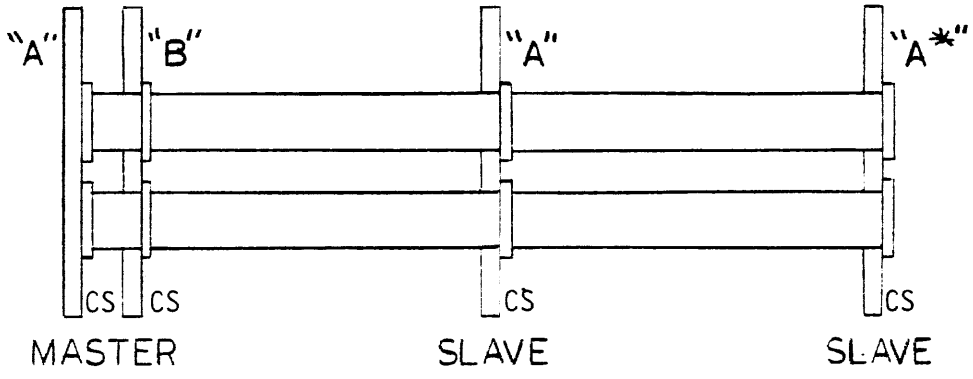
Bracketed signals are open at the formatter, connected at the transport only.

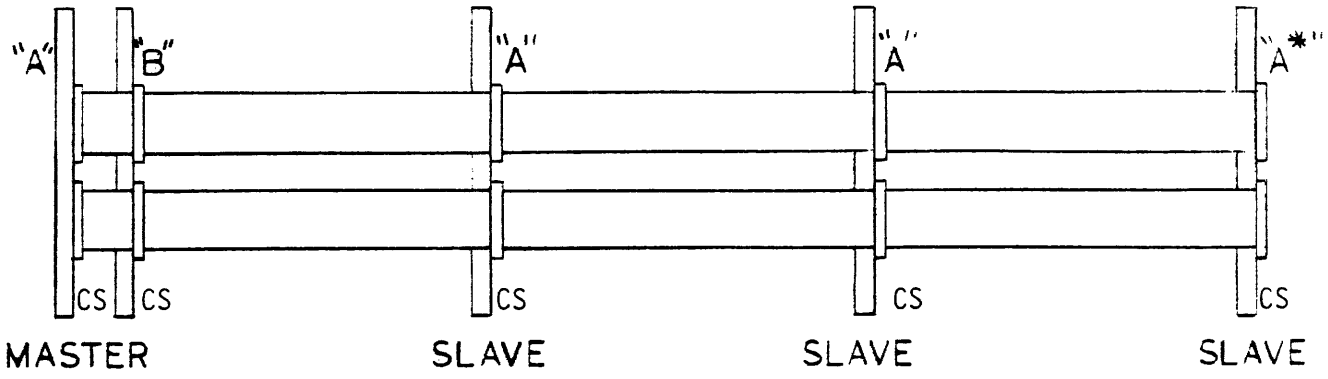
Figure 2-4, Transport I/O



NUMBER OF TRANSPORTS	CABLE NUMBER
ONE	2051579-0001
TWO	2051579-0002
THREE	2051579-0003
FOUR	2051579-0004







CS = Component side of P.C. Card Ass'y.

* Termination Packages U3, U52, and U53, must be installed only on the Write/Control Card of the last transport in the Daisy-Chain.

FIGURE 2-5, TRANSPORT DAISY-CHAINING

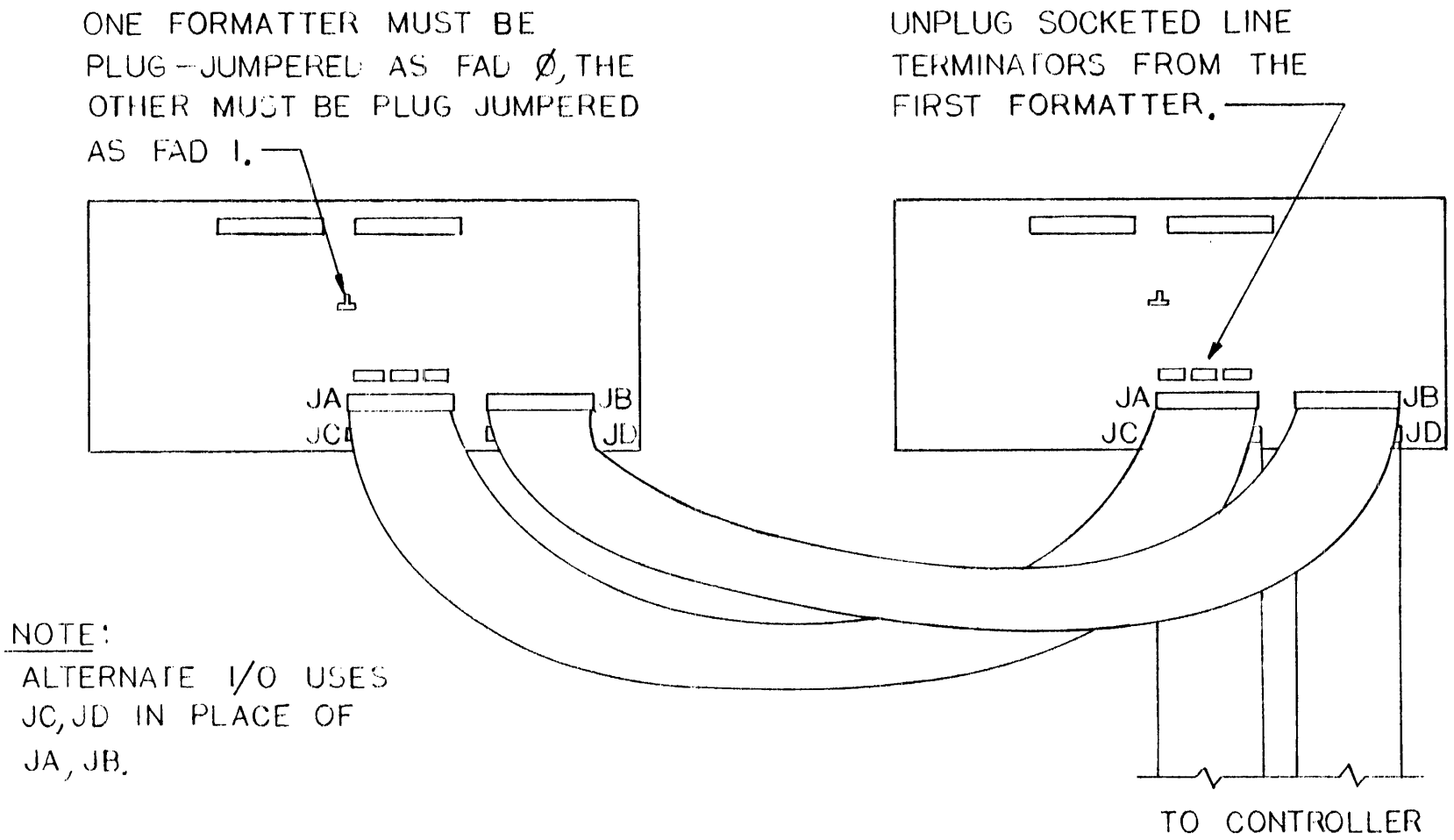


FIG 2-6, DAISY-CHAINED FORMATTERS.

3 - OPERATION

3.1 INTRODUCTION. This section explains each basic operation performed by the formatter and describes the interface signals and tape formats.

3.2 BASIC OPERATIONS. Basic tape operations controlled by the formatter are shown in chart form in figure 3-1. These operations are initiated with a low (true) pulse on the GO interface line. Three operations in addition to the sixteen listed in this chart, "Rewind", "Off Line", and "Load and On Line", are executed directly by the selected transport without tying up the formatter. The direct commands are described in paragraph 3.6.5.

3.2.1 WRITE. When executing a write command, the formatter first accelerates the tape, then, following an appropriate delay, begins to transfer write data from the controller to the tape transport. Data transfer ends when the signal "Last Word" (LWD) is received from the controller. If the transport is equipped with a dual gap head, tape is not decelerated until the entire record has been read; if equipped with a single gap head, tape is decelerated immediately. Different prerecord delays assure proper interrecord gap length. Writing may be done "on-the-fly" if so desired by issuing a new GO after the trailing edge of DBY.

3.2.2 EDIT. The edit (or overwrite) operation is identical to the write operation except that the transport's write current is allowed to decay immediately after the last character is written while the tape is still at full speed to avoid creating a turn-off glitch in the interrecord gap. Before overwriting a record the controller must always space or read reverse over that record with EDIT true. This ensures the proper placement of the new record on tape.

3.2.3 WRITE FILE MARK. The write file mark operation is executed by the formatter without controller involvement. Both the NRZ and phase encoded file marks (EOF) are preceded by a 4.8 inch erased gap.

3.2.4 ERASE. There are three different erase operations.

a) Variable Length Erase. This operation is identical to the write operation except that no write strobes (WDS) are supplied to the transport. The controller, however, is supplied with write strobes (WSTR), and by counting these it determines when to assert LWD to end the erasure.

b) Fixed Length Erase. This operation erases 4.8 inches of tape.

c) Delete. This operation is identical to the variable length erase except that the transport's write current is allowed to decay while the tape is still at full speed to avoid creating a glitch in the interrecord gap.

3.2.5 READ FORWARD. When executing a read forward command the selected transport is accelerated and then the formatter reads one record from tape. When the following gap is detected, tape is decelerated. Records may be read "on-the-fly" by issuing a new GO after the trailing edge of DBY. In

OPERATION:	SIGNALS REQUIRED:				
	REV	WRT	ERASE	WFM	EDIT
Write		X			
Overwrite(edit)		X			X
Write EOF		X		X	
Erase (variable length)		X	X		
Erase (fixed length)		X	X	X	
Delete (edit)		X	X		X
Read Forward Record					
Read Reverse Record	X				
Space Forward Record			X		
Space Reverse Record	X		X		
Read Forward File				X	
Read Reverse File	X			X	
Space Forward File			X	X	
Space Reverse File	X		X	X	
Read Reverse (edit)	X				X
Space Reverse (edit)	X		X		X

FIGURE 3-1, PERMISSIBLE TAPE OPERATIONS

NRZ check character(s) are distinguished from the data by a low (true) level on the CCG line. The check character(s) may be truncated in the formatter, if so desired, by placing the CHECK CHARACTER plug jumper in position WP. See paragraph 1.5.2.

3.2.6 READ REVERSE. The read reverse operation is identical to the read forward except that the sequence of characters is, of course, reversed. When reading reverse with EDIT true, the postrecord delay is slightly extended so that the tape is optimally positioned for a subsequent overwrite operation. In NRZ, the 9 track NRZ check characters are identified by a true level on the CCG line. Their transfer may be suppressed placing the CHECK CHARACTER plug jumper in position WP. See paragraph 1.5.2.

3.2.7 SPACE FORWARD RECORD and SPACE REVERSE RECORD. The Space Record operations are similar to Read operations. Data is read from the transport by the formatter but is not passed to the controller; the read strobe (RSTR) and error indications (HER, CER) are suppressed. File marks, however, are detected and indicated. If BOT is encountered during a space reverse operation the transport stops the tape.

3.2.8 SPACE FORWARD FILE and SPACE REVERSE FILE. When executing the Space File commands the formatter automatically reads "on-the-fly" until a file mark (EOF) is encountered. The tape is stopped in the gap following the file mark. Usually no data or error indications (RSTR, HER, CER) are sent to the controller. If EOT is encountered when spacing forward the tape is stopped in the next interrecord gap. If BOT is encountered when spacing reverse the tape is stopped immediately.

3.2.9 READ FORWARD FILE and READ REVERSE FILE. When executing the Read File commands the system automatically reads consecutive records "on-the-fly" until a file mark (EOF) is read. The tape is then halted in the gap following the file mark. The DBY line cycles for each record, going true (low) just before data transfer begins and returning false (high) shortly after data transfer ends. If EOT is encountered while reading forward the tape is stopped in the next interrecord gap. If BOT is encountered while reading reverse the tape is stopped immediately.

3.2.10 ILLEGAL OPERATIONS. In all the following situations the HER and CER flags are both pulsed true (low).

a) GO is issued with REV true when tape is located at BOT.

b) The tape is moved twenty-five feet of tape without encountering data.

c) No data is read while writing with a dual gap transport after the head gap space.

d) GO is issued with <u>both</u> the REV and WRT lines true.

3.3 GAP GENERATION.

3.3.1 INTERRECORD GAP. The formatter provides the timing necessary to generate the required 0.6 inch gap between records on 9 track tape, and the required 0.75 inch gap between records on 7 track tape.

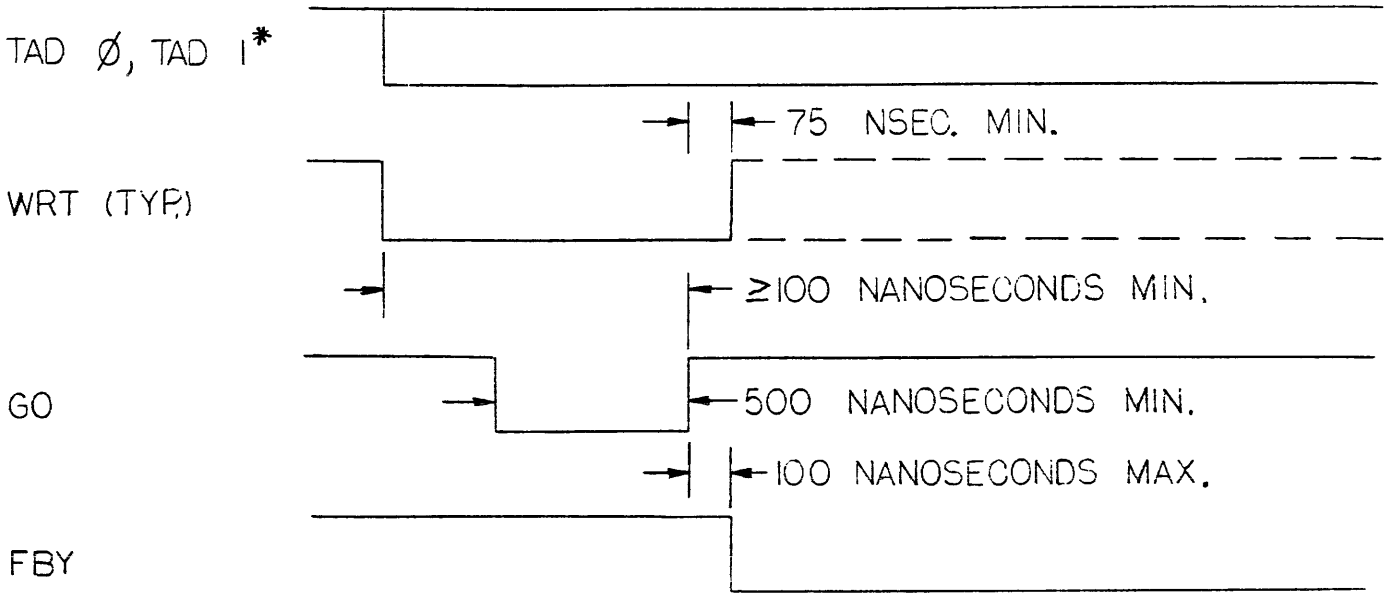


FIGURE 3--2, CONTROL WAVEFORMS

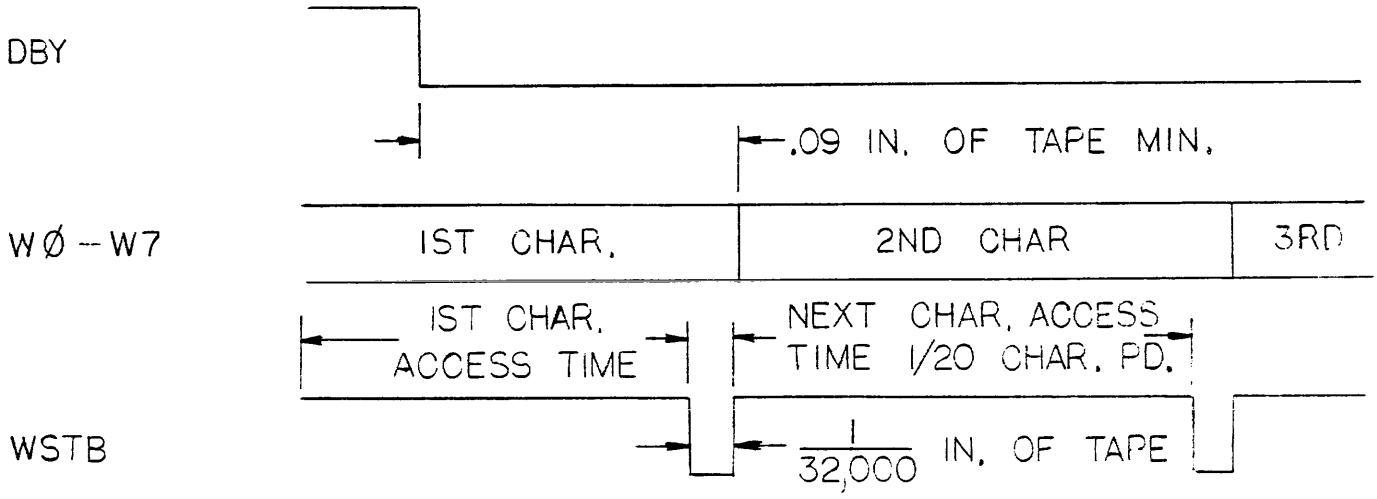


FIGURE 3-3, WRITE DATA WAVEFORMS

*IF TRANSPORT STATUS USED TO CONDITION OPERATION GO SHOULD NOT OCCUR UNTIL STATUS FROM SELECTED TRANSPORT IS VERIFIED.

3.3.2 INITIAL GAP. When writing in NRZ, the first record is written approximately 4.8 inches after the trailing edge of the BOT marker. In PE, the ID burst is written alongside the BOT marker, extending .8 inches past its trailing edge; a 4.0 inch gap is generated before the first record, placing the first record again 4.8 inches from the trailing edge of the BOT marker. This operation must occur from load point or following a rewind after reading. See the Transport Manual for BOT position information.

3.3.3 FILE MARK GAP. A file mark (EOF), except from BOT, is preceded by a total gap of 4.8 inches in both NRZ and PE.

3.4 PHASE ENCODED FORMAT. The formatter and -40 series transport write tapes in accordance with ANSI Interchangeability Specification No. X3.39-1973 for 9 track 1600 cpi recording.

Phase encoded data records are characterized as follows:

a) A zero bit is a transition in the center of the bit cell out of the direction of gap erasure magnetization, corresponding to a false-to-true (high-to-low) transition on a formatter-to-transport write data line.

b) A one bit is a transition in the center of the bit cell into the direction of gap erasure magnetization, corresponding to a true-to-false (low-to-high) transition on a formatter-to-transport write data line.

c) Because a one bit and a zero bit are defined as flux changes in a specified direction, an additional transition is required at the cell boundary when successive one or zero bits are written. This transition is referred to as the phase transition and is in the direction opposite to that of the data transition.

A data record on tape is comprised of three parts: the preamble, the actual data, and the postamble. These are illustrated in figure 3-6.

The preamble precedes the data portion of the record and consists of 40 zero bits in all tracks followed by a single one bit in all tracks. When reading, the formatter uses the preamble to synchronize the decoding circuits.

The actual data portion of the record may contain any number of characters. The ANSI Interchangeability Specification calls for 18 to 2048 characters, but the formatter and -40 series transport operate from one to the physical limit of the tape.

The postamble immediately follows the data field. It consists of a single one bit in all tracks followed by 40 zero bits in all tracks. The postamble permits the formatter to detect the end of the data field and to synchronize the decoding circuits when reading in reverse.

The parity bit is generated by the formatter such that the number of one bits in any character in the data field is always odd. Internal parity generation may be suppressed by asserting the GATE WP line. External parity may then be supplied on the WP/C line. See paragraph 1.5.3 .

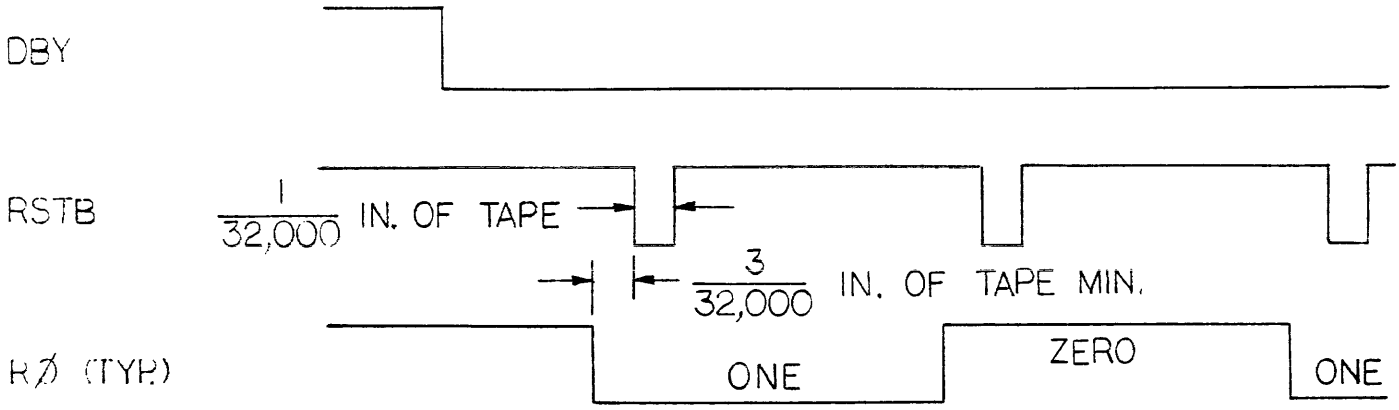


FIGURE 3-4, READ DATA WAVEFORMS

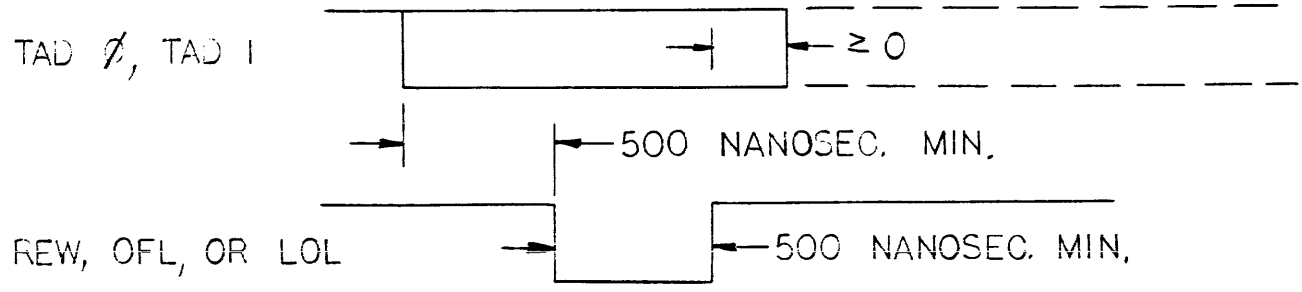


FIGURE 3-5, DIRECT COMMAND WAVEFORMS

When writing or erasing from BOT, the formatter automatically records the required identification (ID) burst alongside the BOT marker. The ID burst consists of alternating one and zero bits (i.e. 1600 frpi) in track P only; the other eight tracks are dc erased. To properly locate the ID burst with respect to the BOT marker, the write/erase command from BOT must be preceded by a rewind from off the BOT marker or by a load operation, not by a read/space reverse operation.

When reading from BOT or writing with a dual gap head, the formatter looks for activity in all tracks. If track P alone is active the IDENT interface line is pulsed low.

When a write-end-of-file command is executed the formatter creates the required extended gap erasure and then writes 128 zero bits (3200 frpi) in tracks 2, 6, and 7. Tracks P, Ø, 1, 3, 4, and 5 are dc erased. When reading, the formatter recognizes an EOF if there are at least 64 transitions (32 cells) in tracks 2, 6, and 7 and tracks 1, 3, and 4 are dc erased. According to the standard P, 0, and 5 may contain zero bits or may be dc erased, so these tracks are not tested.

The formatter recognizes a valid preamble if at least eight tracks remain active at 3200 frpi for 15 consecutive cells. After this time a dropout is detected if no transition is present in a track for a time greater than 1-1/3 cells. If only one of the nine tracks drops, the formatter begins correcting that track through the "parity error" indication. When this reconstruction of data in a single track is being performed the interface signal CER goes low. If a dropout is detected in more than one track the transfer of read data ends immediately and the HER line goes low. The tape is not decelerated, however, until after the inter-recofd gap is detected by the absence of transitions in all tracks for 16 cell times.

The HER line is pulsed low when a read data character exhibiting even parity is presented at the I/O.

Since the read deskewing circuits provide four bits of storage in each track, the read data arriving from the transport may be skewed up to three cells without causing an error. Skew in excess of three cells terminates data transfer and sets HER and CER low. Other error conditions detected by the formatter which produce HER and end data transfers are: 1) improper preamble, 2) improper postamble, 3) premature detection, and 4) more than one track dropped.

3.5 NRZ FORMAT. The formatter and -40 series transport in the appropriate configurations write tapes in accordance with ANSI Interchangeability Specifications X3.22-1973 for 9 track 800 cpi NRZ recording and X3.14-1973 for 9 track 200 cpi NRZ recording.

NRZ data records are characterized as follows:

a) A one bit is a flux reversal in the middle of the bit cell on tape. The direction of the transition is not significant; only its presence (or absence) is important. A one bit corresponds to a low (true) level on the write data interface line.

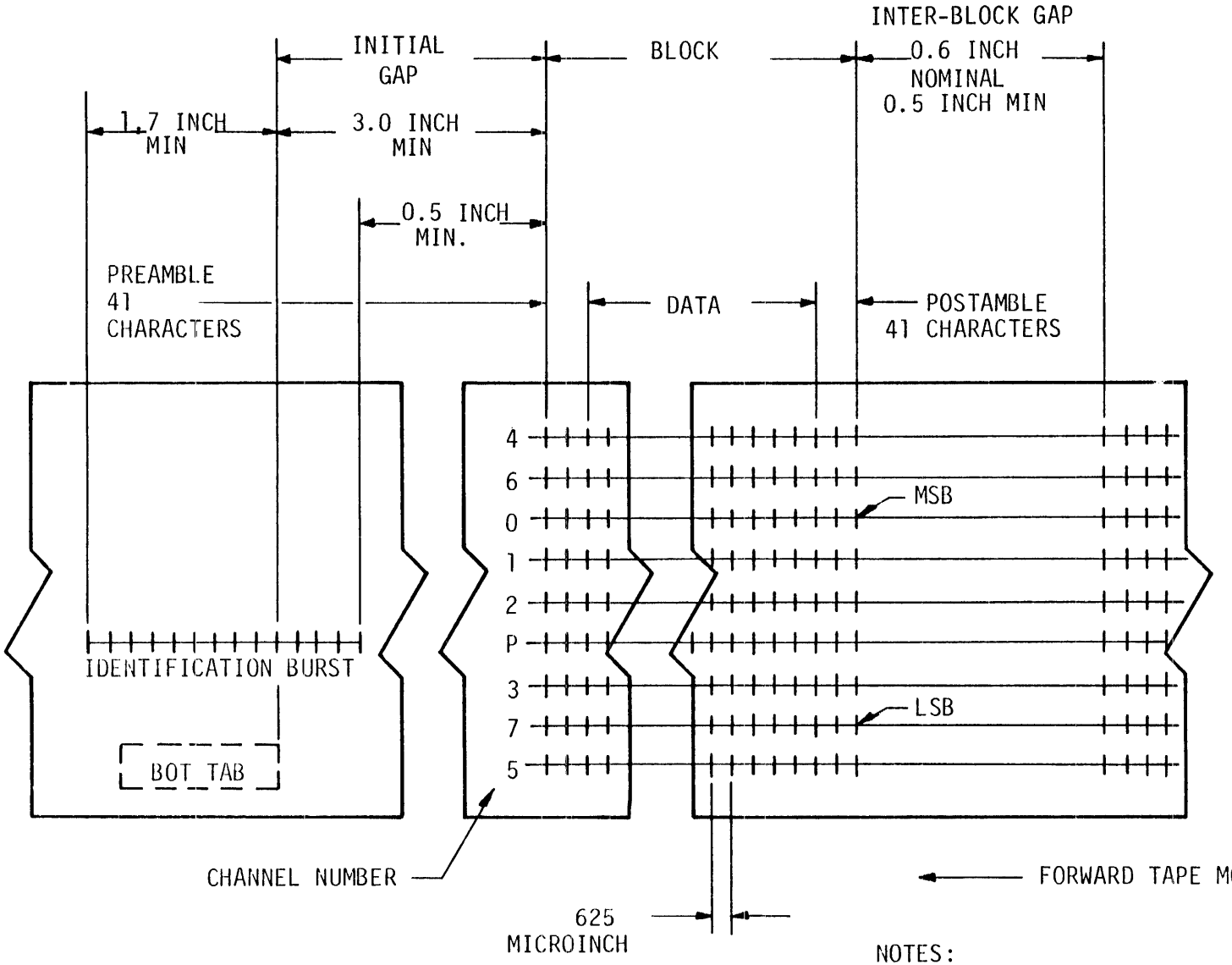


FIGURE 3-6 , 9 TRACK PHASE ENCODED TAPE FORMAT STANDARD

NOTES:

1. TAPE IS SHOWN WITH OXIDE SIDE UP.
2. TAPE IS TO BE FULLY SATURATED IN THE ERASED DIRECTION IN THE INTER-BLOCK GAP AND THE INITIAL GAP.
3. THE IDENTIFICATION BURST MUST EXTEND PAST THE END OF THE BOT MARKER.

b) A zero bit is the lack of any flux reversal in the bit cell on tape; this corresponds to a high (false) level on the write data interface line.

These are illustrated in figures 3-7 and 3-8.

A NRZ data record or block consists of 18 to 2048 ASCII characters according to the ANSI Interchangeability Specification. The formatter, however, has no hardware limitation restricting record size, so any length record from one character to the full length of the tape may be read or written.

The formatter permits 7 track NRZ tapes to be written and/or read at 200, 556, and 800 cpi with either odd or even parity. Note that although 9 track tapes are normally written only at 800 cpi and only with odd parity, the formatter reads and writes 9 track tapes with even or odd parity at both 200 and 800 cpi.

When even parity tapes are being written the formatter automatically converts an all zeroes data character to 001010 or 00001010. (A NRZ character must contain at least one one bit to be recovered from the tape by the transport's read circuits.)

The formatter generates the cyclic redundancy check character (CRCC) for 9 track 800 BPI tapes. When reading, the formatter regenerates the CRCC from the data and checks it bit-for-bit against the CRCC read from tape. A mismatch is indicated on the HER line.

The formatter generates the WARS pulse which clears the transport's write register to record the longitudinal redundancy check character on both 7 and 9 track tapes. Recording the LRCC makes the number of one bits in each track even, returning the direction of magnetization in each track to the proper direction for gap erasure. When reading, the formatter checks the LRCC bit-for-bit and indicates an error on the HER line.

When executing a Write-EOF command the formatter erases the required extended gap and then records a one character record with its associated LRCC. For 7 track tape the character is 001111 with a false parity bit; for 9 track 800 BPI tape the character is 00010011 and the CRCC is all zero bits. In both cases the LRCC is identical to this file character.

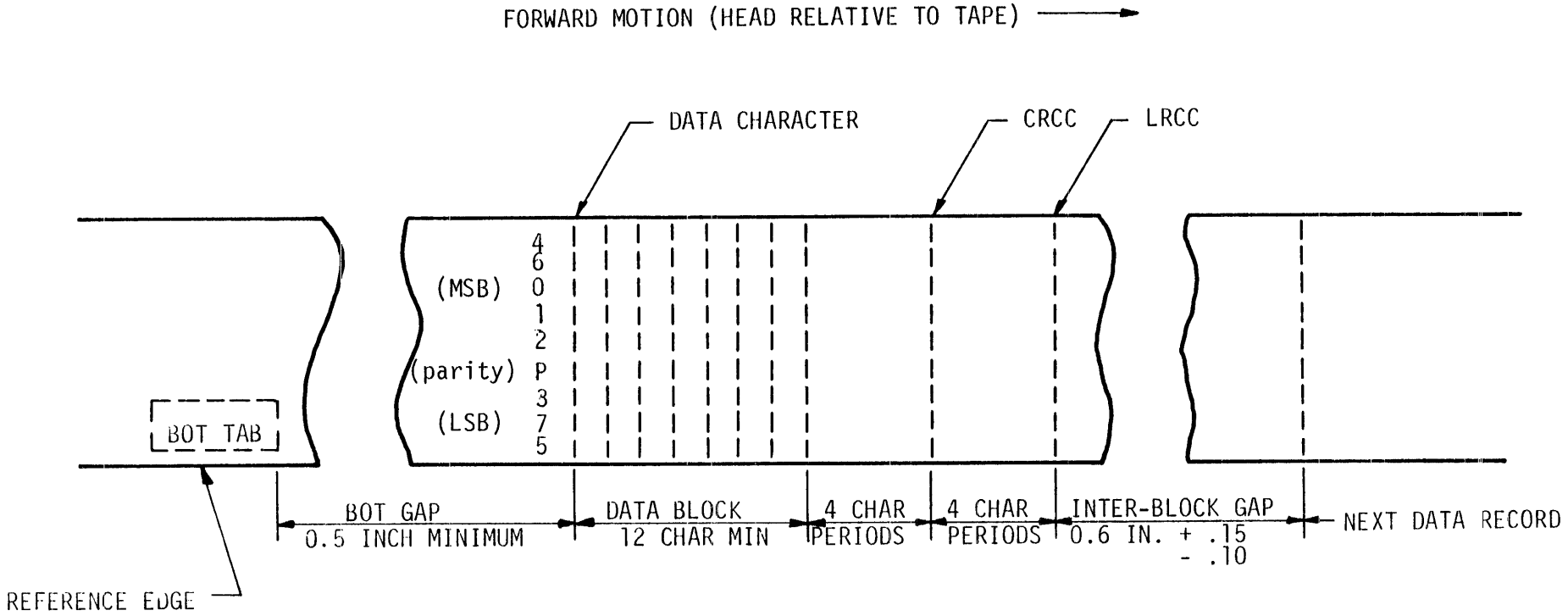
3.6 INPUTS.

3.6.1 STATIC CONTROL LINES.

FEN, Formatter Enable. This line must be held true (low) for all operations; a false level or pulse clears the formatter(s).

FAD, Formatter Address. This line must match the setting of the FAD plug jumper on the formatter card to select a tape unit. True (low) selects FAD1, false selects FADØ. See paragraph 1.5.4 to establish the formatter's address(es).

TADØ, Tape Address MSB; TAD1, Tape Address LSB. These two lines are decoded by the formatter to select one of four daisy-chained transports.



NOTES:

1. TAPE SHOWN WITH OXIDE SIDE UP.
2. CHANNELS 0 THROUGH 7 CONTAIN DATA BITS IN DESCENDING ORDER OF SIGNIFICANCE.
3. DATA PACKING DENSITY IS FIXED AT 800 CHARACTERS PER INCH.

FIGURE 3-7 9 TRACK NRZI FORMAT

TADØ	TAD1	SELECT TAPE UNIT
False (high)	False (high)	Ø
False (high)	True (low	1
True (low)	False (high)	2
True (low)	True (low)	3

GATE WP, Gate Write Parity. When this line is held false (high) the formatter generates vertical parity internally for each character; when held true the formatter accepts the externally generated parity provided by the controller on the WP/C input line. In lieu of this input line a plug jumper may be used (See paragraph 1.5.3). Digi-Data interface only.

SPD SEL, Speed Select. This line is active only when the formatter is addressing a dual speed transport. A true (low) level selects the optional tape speed, and a false level selects the normal speed. Digi-Data interface only.

3.6.2 CONTROL LINES SAMPLED AT "GO" TIME.

REV, Reverse. This line false (high) at GO time results in forward tape motion; true results in reverse tape motion. Writing/erasing are illegal in the reverse direction. (See paragraph 3.2.10 regarding illegal operations.)

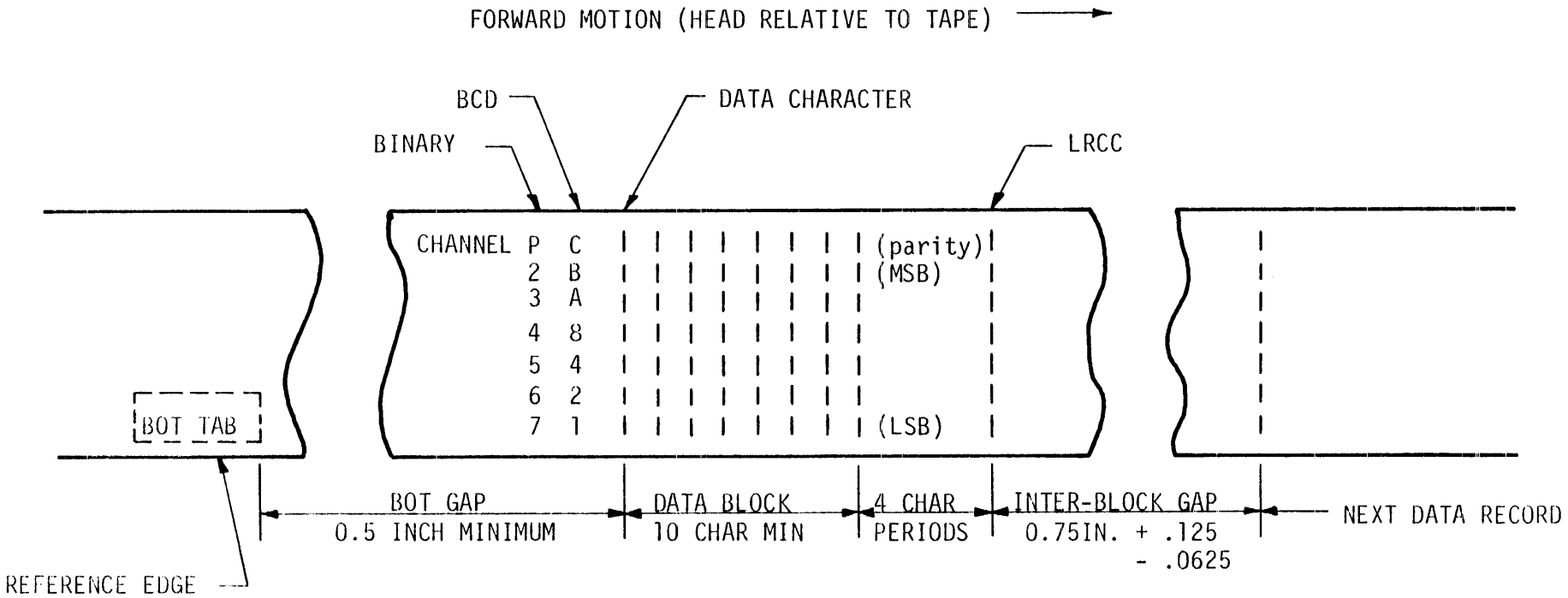
WRT, Write. This line true (low) at GO time activates the transport's write current; false results in a read only operation. A write operation is terminated when LWD is issued. A read operation automatically terminates after a record is read.

WFM, Write File Mark. If this line and WRT are both true (low) at GO time, an EOF will be written on tape with an extended gap preceding it. If WRT, WFM, and ERASE are all true a fixed length erasure of 4.8 inches will occur. If WFM is true but WRT is false at GO time a search-to-EOF operation will commence, either in the forward or reverse direction as specified by REV. Tape motion in this last case does not cease until an EOF is read or BOT/EOT is encountered.

ERASE, Erase. If this line and WRT are both true (low) at GO time, an erase operation results. This variable length erase is terminated as are write operations. If ERASE is true (low) but WRT is false (high) at GO time, the addressed tape unit will space forward (or reverse) one record; this is a normal read operation except that the read strobe (RSTR) and the error flags (HER and CER) are suppressed. (ERASE true (low) during the space-to-EOF operation described above is not required but may be desired.)

EDIT, Edit. This line performs two distinct editing functions.

a) Immediately prior to overwriting a record, that record should be read in reverse with EDIT true (low). The formatter will extend the postrecord delay slightly to achieve optimum head/tape position for the subsequent overwrite.



NOTES:

1. TAPE SHOWN WITH OXIDE SIDE UP.
2. CHANNELS 2 THROUGH 7 CONTAIN DATA BITS IN DESCENDING ORDER OF SIGNIFICANCE.
3. DATA PACKING DENSITY MAY BE 200, 556 or 800 CHARACTERS PER INCH.

FIGURE 3-8 7 TRACK NRZI FORMAT

b) If this line and WRT are both true (low) at GO time, the transport will turn off its write current while the tape is still at synchronous speed immediately after the last character is recorded to avoid creating a turn-off glitch in the inter-record gap.

THR1, High Read Threshold. This line true (low) at GO time decreases the sensitivity of the transport's read discrimination circuits; this is useful when verifying the fidelity of freshly recorded tapes. False selects the normal clip level. (This line is ignored by -40 series transports.)

THR2, Low Read Threshold. A true (low) level at GO time during a read operation increases the sensitivity of the read discrimination circuits; this is useful when attempting to recover severely degraded data. False selects the normal clip level.

PAR, Even Parity. This line true (low) at GO time generates and/or verifies even parity tapes during 7 or 9 track NRZ operations. When writing even parity tapes the formatter automatically converts Ø's to A's. False level selects odd parity. Digi-Data interface only.

DEN, Low Density Select. This line true (low) at GO time selects low density, i.e. 800 BPI on 9 track NRZ/PE transport, or the lowest available density (either 200 or 556 BPI) on 7 or 9 track dual density NRZ transports. False selects high density, i.e. 1600 BPI on 9 track NRZ/PE transports, or the highest available density (either 556 or 800 BPI) on 7 or 9 track dual density NRZ transports. (FAD may alternately be used to select transport density; see paragraph 1.5.5.)

3.6.3 CONTROL PULSES.

GO, Initialization Pulse. This low true pulse causes the formatter to sample the control lines described above, and subsequently to execute the specified operation. Minimum pulse width is 500 nanoseconds; the control lines must be stable 100ns prior to the trailing edge of GO and remain stable for 75ns. If the formatter uses transport RDY as a clear in place of power up, the user must select the transport and test RDY before sending GO. If this is not done the formatter might be cleared by RDY going false as the transport is selected, thus blocking GO.

LWD, Last Word. This low true pulse or level indicates the end of data transfer during a write data operation. LWD may occur either synchronously (coincident with the last data character, spanning the last required WSTR) or asychronously (within one-half character period after the last required WSTR), depending on the position of the LWD plug jumper (see paragraph 1.5.1).

3.6.4 WRITE DATA LINES.

WØ thru W7, Write Data Ø thru 7. These eight lines transmit write data from the controller to the formatter; low specifies one, high specifies zero. These lines must remain stable for the duration of each WSTR. The first character must be presented before the leading edge of the first WSTR; subsequent characters must be presented within 95% of a character period after the trailing edge of WSTR. W7 is the least significant bit. WØ and W1 are not used in seven-track operations.

WP, Write Parity. This input line is active only when external parity is selected. The controller must provide the write data parity bit on this line coincident with the write data character on lines WØ-W7. With GATE WP false, as is normally the case, the formatter generates parity internally.

3.6.5 DIRECT COMMAND LINES. See figure 3-5 for direct command waveforms. All signals are routed directly to the transport so that the formatter does not become "busy." The minimum pulse width for these signals is 500 nanoseconds.

REW, Rewind. A true (low) pulse causes the selected transport to rewind its tape to the load point.

OFL, Off Line. A true (low) pulse causes the selected transport to be removed from remote control.

LOL, Load and On Line. A true (low) pulse causes the selected transport to apply tension to the tape and to go On Line. Only one pulse is required; any subsequent pulses will place the transport alternately off and on line.

3.7 OUTPUTS

3.7.1 TRANSPORT STATUS AND CONFIGURATION LINES.

NRZ, NRZ. True (low) level on this line indicates that the selected transport is set to write/read NRZ tapes. False (high) indicates a phase encoded transport.

SGL, Single Gap Head. True (low) level on this line indicates that the selected transport is equipped with a single gap head. False level indicates a dual gap head.

SPEED, Low Speed. This line is high at all times. Alternate I/O only.

7 TRK, Seven Track. True (low) on this line indicates that the selected transport is a 7 track unit; false indicates 9 track. Digi-Data interface only.

RDY, Ready. True (low) level on this line indicates that the selected transport is on line, not rewinding, and loaded with tape, i.e., ready to execute a command. Operations should not be attempted using a transport which is not ready.

ONL, On Line. True (low) level on this line indicates that the selected transport is under remote control; false indicates that the transport has been removed from remote control.

RWD, Rewinding. True (low) level on this line indicates that the selected transport is performing a rewind operation.

FPT, File Protected. True (low) level on this line indicates that the selected transport is loaded with a reel of tape not containing a write enable ring and consequently that write/erase operations cannot be executed. False level indicates that writing and erasing are permitted.

LPT, Load Point. True (low) level on this line indicates that the selected transport is loaded with tape positioned at the BOT marker.

EOT, End of Tape. True (low) level on this line indicates that the selected transport is sensing the EOT marker.

DEN STAT, Density Status. True (low) level on this line indicates that the selected transport is operating at 200, 556, or 1600 BPI. False indicates operation at 800 BPI. Digi-Data interface only.

3.7.2 FORMATTER INDICATIONS.

FBY, Formatter Busy. This line goes true (low) on the trailing edge of GO and remains true until after the command has been executed and tape motion has ceased. (When back spacing into BOT, it is cleared shortly after sensing BOT along with all other outputs from the formatter.)

DBY, Data Busy. This line goes true (low) after the prerecord delay (acceleration), indicating that the formatter is about to begin writing to or reading from tape. This line returns false just before tape is decelerated. When executing "on-the-fly" operations a new GO may be issued after the trailing edge of DBY if the WRT and REV control lines are not changed; if the lines are changed a new GO must not be issued until FBY returns false.

CCG, Check Character Gate. NRZ signal only. This signal envelops the reading of the NRZ check character(s). When reading forward CCG goes true (low) upon detecting 2½ empty character spaces (cf. NRZ format in paragraph 3.5) and remains true until FBY goes false. In "on-the-fly" operations CCG goes false when the new command is initiated. When reading reverse CCG only occurs in 9 track transports. In reverse CCG goes true with DBY and returns false immediately after both check characters are read. On the alternate I/O, CCG and IDENT, a PE only signal, share the same line.

IDENT, Identification Burst. Phase encoded only. This line pulses true (low) when the identification burst, located alongside the BOT marker, is read. (The IDENT signal is supplied on the CCG line during PE operations on the alternate I/O.)

FMK, End-of-File-Mark. A true (low) pulse on this line indicates that an EOF has been detected. FMK goes true as soon as the EOF is decoded and remains true until DBY goes false.

HER, Hard Error. A true (low) pulse or level on this line indicates that an uncorrectable read error has occurred. Generally a pulse on this line indicates a parity error, and a level a format error. In the latter case, read data transmission ceases for that record. HER is also true for illegal commands.

CER, Corrected Error. Phase encoded only. This line true (low) indicates that a single channel has been lost and is being reconstructed by the disabled "parity error" for the remainder of that record. CER is also true for illegal commands.

3.7.3 DATA CLOCKS AND DATA.

WSTR, Write Strobe. A true (low) pulse lasting longer than 400 nanoseconds (31.25 microinches of tape) indicates that the write data lines (WØ-W7, WP) have been copied into the formatter. The next data character to be written should be placed on the write data lines within 95% of a character period of the trailing edge of WSTR.

RSTR, Read Strobe. A true (low) pulse lasting longer than 400 nanoseconds (31.25 microinches of tape) indicates that a new character is available on the read data lines (RØ-R7, RP). Either edge of RSTR may be used to sample the data.

RØ-R7, RP, Read Data Channels Ø true 7 and Parity. These nine lines transmit read data from the formatter to the controller; low indicates a one, high indicates zero. Data is generally stable on the lines for a full character period. Bursts of two or three characters may be presented at twice the nominal transfer rate in NRZ and in all read-after-write modes due to timing variations and the formatter's characteristics. R7 is the least significant bit. RØ and R1 are not used in seven-track operations.

4 - BLOCK DIAGRAM DESCRIPTION

4.1 INTRODUCTION. This section describes the formatter's operation in terms of block diagrams figures 4-1, 4-2, and 4-3), the circuit schematics (located at the rear of this manual) and the assembly program listing (not included). Figure 4-5 at the end of this section lists timings for most formatter operations. Troubleshooting procedures are not directly related to actual in-system operation, so it is not necessary to know this section in detail to sucessfully maintain the formatter.

4.2 BASIC ELEMENTS. All motion timing and data transfer are directly controlled by the microprogram. The only function accomplished independent of the processor is decoding/deskewing PE read data (schematic sheets 6, 7, and 8). The microprocessor (schematic sheet 1) consists of two cascaded bi-polar four-bit slices. The microprogram is stored in four 1024 x 8 bi-polar PROMs (sheet 2) and contains of approximately 800 32-bit microinstructions. (The NRZ only and PE only programs are stored in four 512 x 8 PROMs.) The microinstructions addressed by the program sequencer appear on the formatter's 32-bit control-bus. The sequencer provides up to four levels of conditional branching and nesting of subroutines.

Two key elements in the processor itself are the sixteen-word two-port RAM and the high speed arithmetic logic unit (ALU). The formatter's D-bus is the direct data input to the ALU. The ALU/RAM outputs are the formatter's Y-bus. Generally data transfers move information from the D-bus to the Y-bus.

4.3 BIT INPUT AND BIT OUTPUT LOGIC. The bit input logic (schematic sheet 1) allows a microinstruction to test (for 1 or Ø) any one of 32 input bits derived from the tape transport, the controller, and various internal circuits. The bit output logic (sheet 3) allows a microinstruction to set or clear any one of 24 output bits - 5 to the tape transport, 10 to the controller, and 9 to control various internal functions.

4.4 WORD INPUT AND WORD OUTPUT LOGIC. The word input logic gates one of six possible inputs onto the 9-bit wide D-bus. (The ninth bit is transferred via the bit test/set logic.) These six are:

a) the controller write data lines, WØ-W7, WP (sheet 3);

b) the controller command lines, WRT, WFM, EDIT, ERASE, and REV, plus several FLAG bits (sheeet 3);

c) the tape transport NRZ read data lines, RDØ-RD7, RDP (sheet 4);

d) the output of the phase encoded read deskewing circuits (sheets 6, 7, and 8);

e) the status, i.e. the INACTIVE signal, of each phase encoded read channel (sheets 6, 7 and 8);

f) a literal value from the control bus, e.g. the creation of a file mark (sheet 3).

As previously stated, the D-bus is the direct data input to the microprocessor and can be passed through the microprocessor to the Y-bus. The D-bus is also monitored by a 512 x 4 PROM which determines PE "activity" and generates and/or verifies vertical parity.

The word output logic (sheet 2) allows the program to move the data on the Y-bus to either:

a) the controller read data lines, RØ-R7, or
b) the tape transport write data lines, WDØ-WD7.

Since the microprocessor and, consequently, the Y-bus are only eight-bits wide, the parity channel is moved through the bit input/output logic.

4.5 SYSTEM CLOCK AND MOTION CONTROL. Basic formatter timing is provided by a 14.4 MHz crystal oscillator (sheet 5). This master clock is normalized to the selected tape transport's speed to form the processor clock (PROCCLK) at the frequencies listed below:

Tape Speed	Frequency	Divide Master by
75 IPS	4.8 MHz	3
45 IPS	2.88 MHz	5
37.5 IPS	2.4 MHz	2 and 3
25 IPS	1.6 MHz	9
18.75 IPS	1.2 MHz	2 and 6
12.5 IPS	0.8 MHz	2 and 9

The processor clock occurs once for each 15.625 microinches of tape traversed at synchronous speed; moving one inch requires 64,000 processor clocks. Several RAM locations are presettable counters decremented in program loops to achieve proper character spacing for the various tape densities and correct gap length for the various operations. The number of processor clocks per character period is a function of data density.

Density	Cycles per cell
1600 BPI	40
800 BPI	80
556 BPI	115
200 BPI	320

Two standard subroutines in varying multiples produce correct gap spacing: "move 0.005 inches" and "move 0.1 inches".

4.6 NRZ READ SEQUENCE. The read data strobe (RDS) from the transport signals that a new character is being presented on the read data lines (RDØ-RD7, RDP). The trailing edge of the read strobe clocks "playback character ready" (PBCHRDY, sheet 5). PBCHRDY forms RDCLK, which clocks the new character into the read input latches (sheet 4). The program checks for the PBCHRDY flag twice during each character period. If this flag does not occur within 25 feet of tape the transport is stopped and the error flags, HER and CER, are set. When the PBCHRDY flag is true the program jumps into a subroutine in order to transfer the character from the tape I/O to the controller I/O.

Control bus bits 7 and 6 specify the source of the word to be transferred, in this case the transport read lines. Bit 7 high produces the signal RDDATA (sheet 3), which in turn forms RDNRZ (sheet 5). RDNRZ enables the output of the read input latches (sheet 4), moving the new character to the D-bus. RDDATA also clears the PBCHRDY flag. The microprocessor moves the character from the D-bus to the Y-bus, leaving it also in RAM register 3 (sheet 1).

Control bus bits 30 and 31 specify the word destination; in this case the controller read lines (both bits are false). These bits steer the next PROCCLK to latch the character on the Y-bus into the read output latch (sheet 2); the character now appears on the controller read lines (RØ-R7).

Control bus bits Ø-4 specify the bit source as the D-bus extension; control bus bits 8-12 specify the bit destination as the read parity line (RP/C).

As the character moves through the formatter it is low true on the tape I/O, high true on the D-bus, low true on the Y-bus (and in R3), and low true on the controller I/O.

Longitudinal parity is checked using R12 and FLAG 1. Each character read is XORed with the contents of this register. After all characters in a record have been read the contents of R12 and FLAG 1 should be 0. If not, hard error (HER) is generated.

As a data record is read, the CRCC is generated to verify the CRCC read from tape at the end of the record. The read CRCC is stored in RAM register 13 and FLAG 2 and is updated with each character transferred.

Next the program verifies that the data character has proper parity: odd or even as specified. GENDPAR, created in the D-bus monitor (sheet 3), must be at the anticipated level or hard error (HER) is indicated to the controller.

Finally the controller read strobe (RSTR, sheet 3) is set and the program returns from this subroutine. RSTR is two processor clocks wide, varying in width from 400 nanoseconds at 75 IPS to 2.5 microseconds at 12.5 IPS.

4.7 NRZ WRITE SEQUENCE. Before writing each character the program determines if LWD is true and, if not, the write data operation commences or continues. The formatter transfers the write data from the controller I/O (WØ-W7) to the tape I/O (WDØ-WD7). It must also determine whether to derive the tape write parity bit (WDP) from the controller I/O bit (WP) or from the internal parity generation circuit. When generating parity internally the formatter must also determine whether the parity should be odd or even.

A microinstruction moves the data from one I/O to the other. Instruction bits 7 and 6, both false, specify the interface write lines as the word source. Bit 6 false also selects the controller write data lines (WØ-W7) through the multiplexers (sheet 3), and bit 7 gates the mux outputs onto the D-bus. The write data is passed through the mux so that is is high true on the D-bus.

Bit 31 false and bit 30 false specify the word destination as TAPE.WRT. The processor transfers the data from the D-bus to the Y-bus, leaving it in RAM R5. Bits 30 and 31 steer the next processor clock to the write data output latch to move the character to the transport I/O (WDØ-WD7). WSTR is then set true to

FIGURE 4-1
FORMATTER
BLOCK DIAGRAM

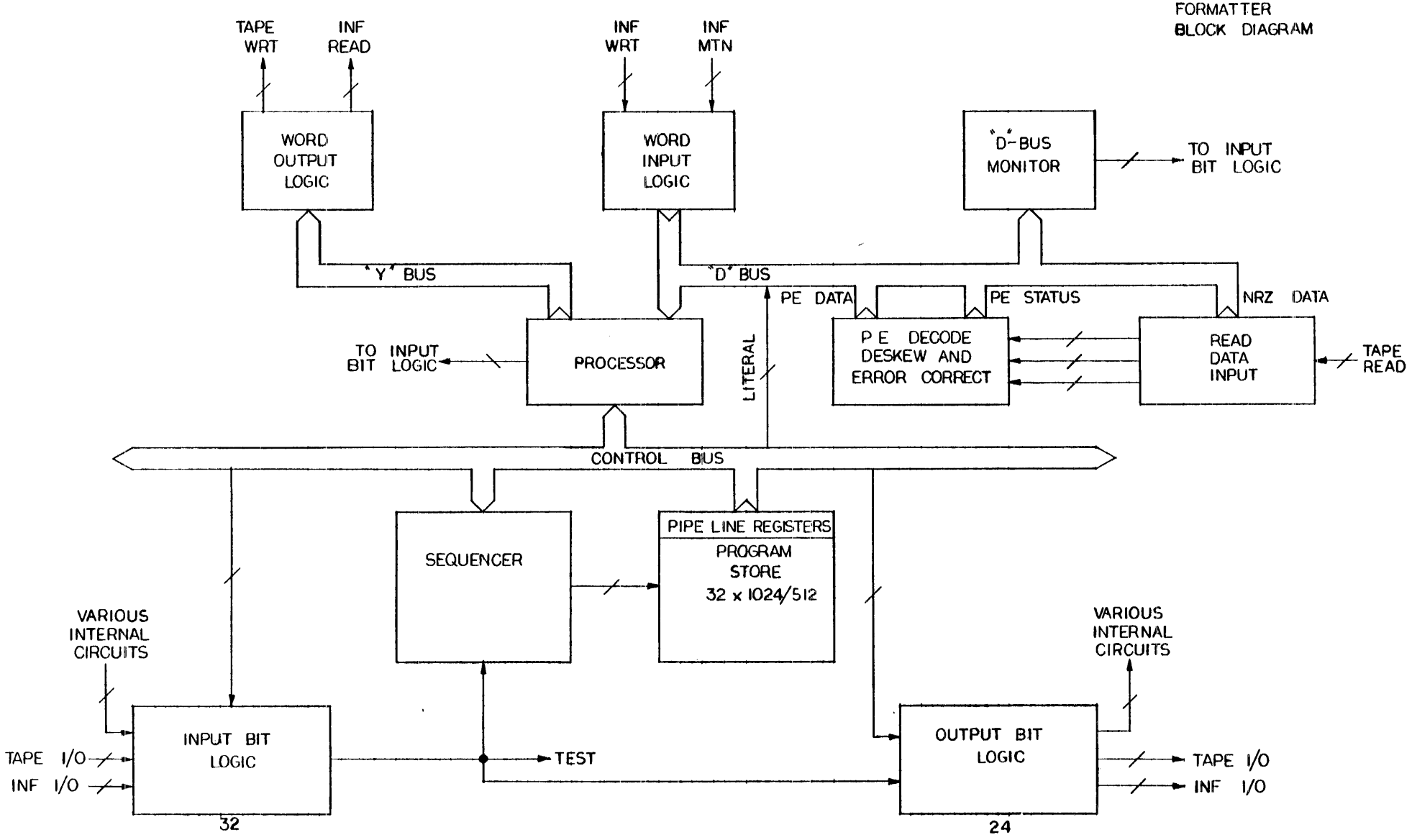
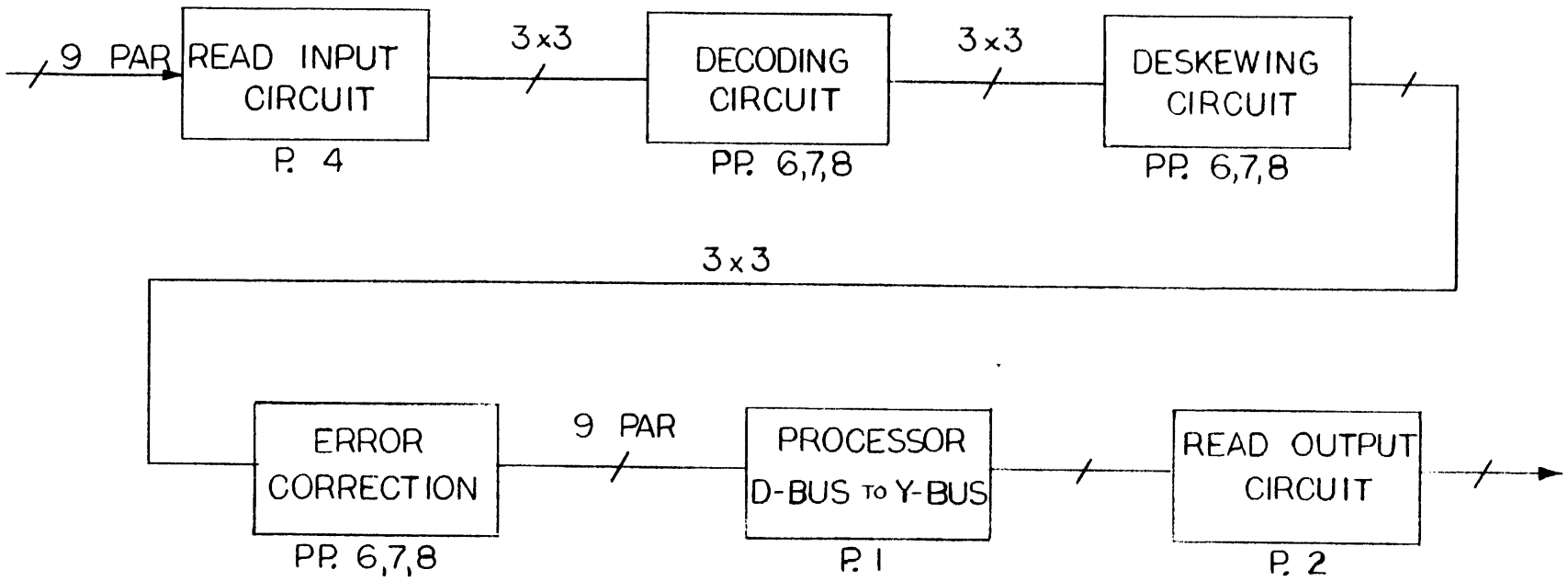


FIGURE 4-2
P. E. READ BLOCK DIAGRAM



indicate to the controller that the write lines can now be changed. The WSTR varies in width from 400 nanosecond to 2.5 microseconds depending on tape speed.

For internal parity generation, the parity bit generated in the D-bus monitor (GENDPAR) is transferred to the tape I/O as WDP.C. If even parity is desired, this bit is inverted. If the selected tape unit is seven-track the two most significant bits are suppressed. The formatter checks for the presence of an "all zeroes" character which must be converted to hexadecimal "A" if internal even parity is being generated.

The processor clock rate is adjusted to tape speed but not to data density. To achieve proper data density when writing to tape, more processor clocks must be used in the 556 and 200 BPI write cycles than in the 800 BPI write cycle. Therefore, twice during each write cycle the processor introduces a "clock correction" routine. Following each adjustment for density the program enters a delay during which the read cycle occurs if a new read character is ready (indicated by PBCHRDY).

Finally the WDS to the transport is set and the program jumps back to the beginning of the write cycle. If LWD is now true the program writes the CRCC from R14 and FLAG 3, and then writes the LRCC by pulsing WARS.

The write cycle is comprised of the following parts:

		800 BPI	556 BPI	200 BPI
A.	Write data transfer	16	16	16
B.	Clock correction to adjust for density.	3	21	123
C.	Delay during which read cycle may occur.	28	27	28
D.	Update CRCC, etc.	9	9	9
E.	Clock correction to adjust for density	3	21	123
F.	Delay during which read cycle may occur	21	21	21
		80	115	320

At 800 BPI the controller WSTR is set on clock 3, but the transport's WDS not until clock 80. The write data character is stable on the transport data lines for almost an entire character period before the strobe occurs. At 800 BPI the test for PBCHRDY occurs on clock 20 and clock 60. The playback data is read and checked as described in paragraph 4.6. If PBCHRDY is not already active by the end of the write operation it must become active within 0.16 inches (0.32 inches for seven-track units) or else the error flags, HER and CER, are set and tape motion is stopped.

4.8 PHASE ENCODED WRITE SEQUENCE. When writing from load point the formatter first accelerates the tape and writes a three-inch ID burst. If the transport is equipped with a dual gap head it also reads this burst; if the ID is not read the tape is stopped and the error flags are set. Following the ID burst four inches of tape are erased, then the program jumps into the normal phase encoded write sequence.

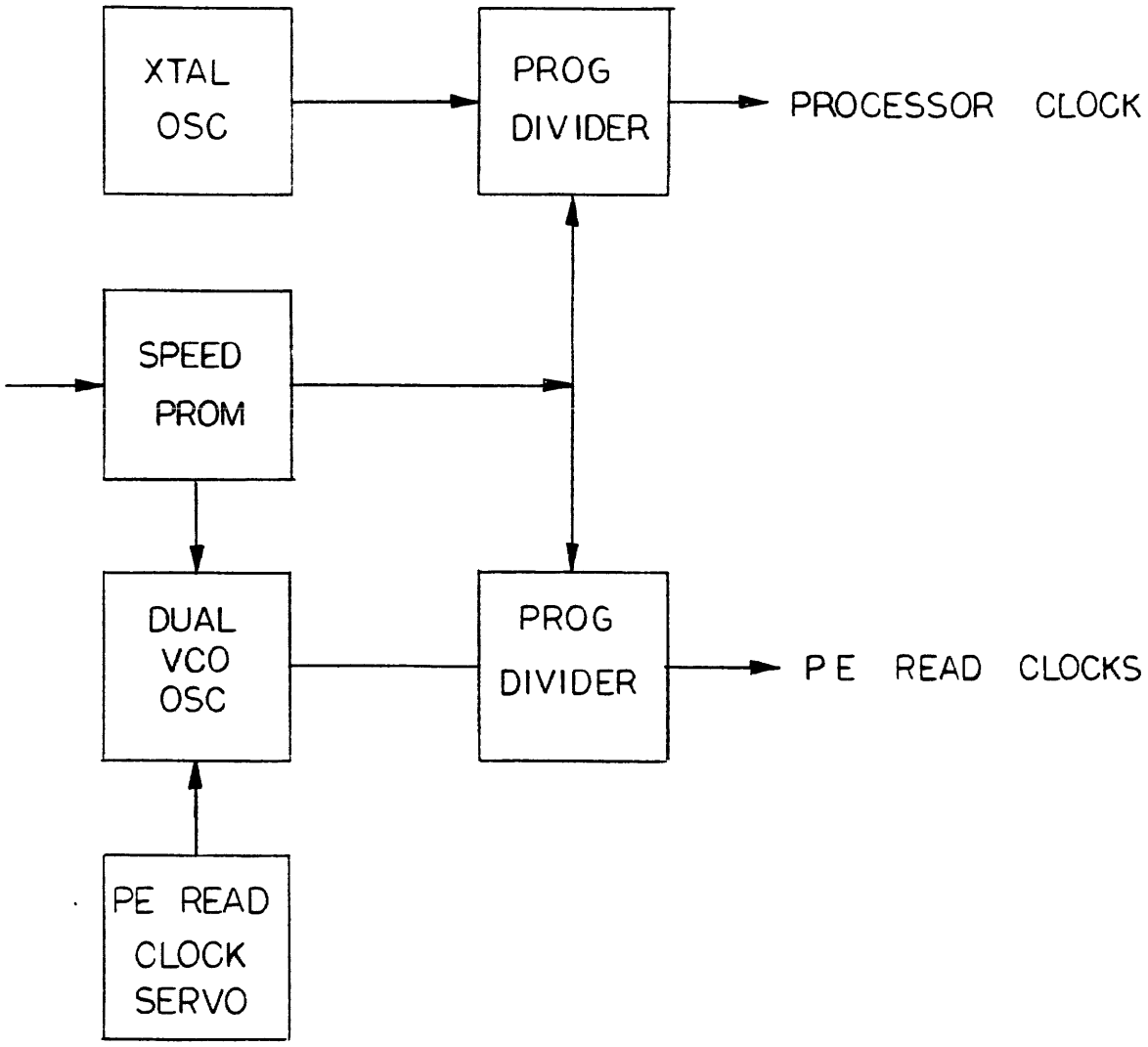


FIGURE 4-3
FORMATTER CLOCKS

The "forty-zeroes" portion of the preamble is written by simply inverting the write data lines (WDØ-7, P) every half cell (i.e. every twenty processor clocks), and providing WDS to the transport. After eighty-one iterations one inversion is skipped (for the preamble "one" phase transition), then the lines are inverted again (for the preamble "one" data transition).

The actual data portion of the record is written next. The recording of each character requires two steps. First the controller write strobe (WSTR) is set, the data move from the controller I/O to the tape I/O through RAM resister 14, and the transport write data strobe (WDS) is set. This step records the phase transition on tape. During the second half of the cell the data stored in R14 are inverted and loaded into the write data lines and a second WDS is supplied to the transport. This records the data transition on tape. During each half cell a delay occurs during which PBCHRDY (read data) can be serviced if necessary. Parity is derived from either the D-bus monitor (GENDPAR) or the controller WP/C input.

When the controller indicates last word (LWD) the formatter generates the postamble. After the postamble is written the program jumps to one of two routines: PEHUNT for 0.16 inches of tape search if the data just written has not yet reached the read stack, or READPE if it has. In single gap transports the program would, or course, simply stop the tape instead of looking for and reading the playback data.

4.9 PHASE ENCODED READ CIRCUITS. When PE data are being read, the transport read data lines are sampled approximately 23 to 24 times each charaacter period. A change from high to low on these lines is a zero; low to high is a one. Whenever a fresh sample differs from the immediately preceding sample a transition is known to have occurred. The read data are multiplexed into three groups of three. Sheets 6, 7, and 8 of the schematic each show one group. Group 1 consists of channels (tracks) 5, 6, and 7; group 2 is channels 0, 3, and 4; group 3 is channels P, 2, and 1. Figure 4-2 is a block diagram of the PE read circuits.

4.9.1 READ TRACKING OSCILLATOR. The PE read tracking oscillator operates around a nominal center frequency of 8.46 MHz. A second tracking oscillator with a nominal center frequency of 4.23 MHz (used only "division by two" transport speeds) may be chosen selected by OSCSEL from the Tape Speed PROM. The output of the tracking oscillator is adjusted to tape speed by a presettable counter to form RDYCLK, which occurs an average of 23.5 times each character period. RDYCLK goes true at the count of 15 and is one clock wide. The frequency of RDYCLK at the various tape speeds is approximately:

Tape Speed	RDYCLK Frequency
75 IPS	2820 KHz
45 IPS	1692 KHz
37.5 IPS	1410 KHz
25 IPS	940 KHz
18.75 IPS	705 KHz
12.5 IPS	470 KHz

Counts of 13, 14, and 15 in the tracking oscillator divider are gated to form three PBCLKs (playback clocks). PBCLK is used throughout the phase

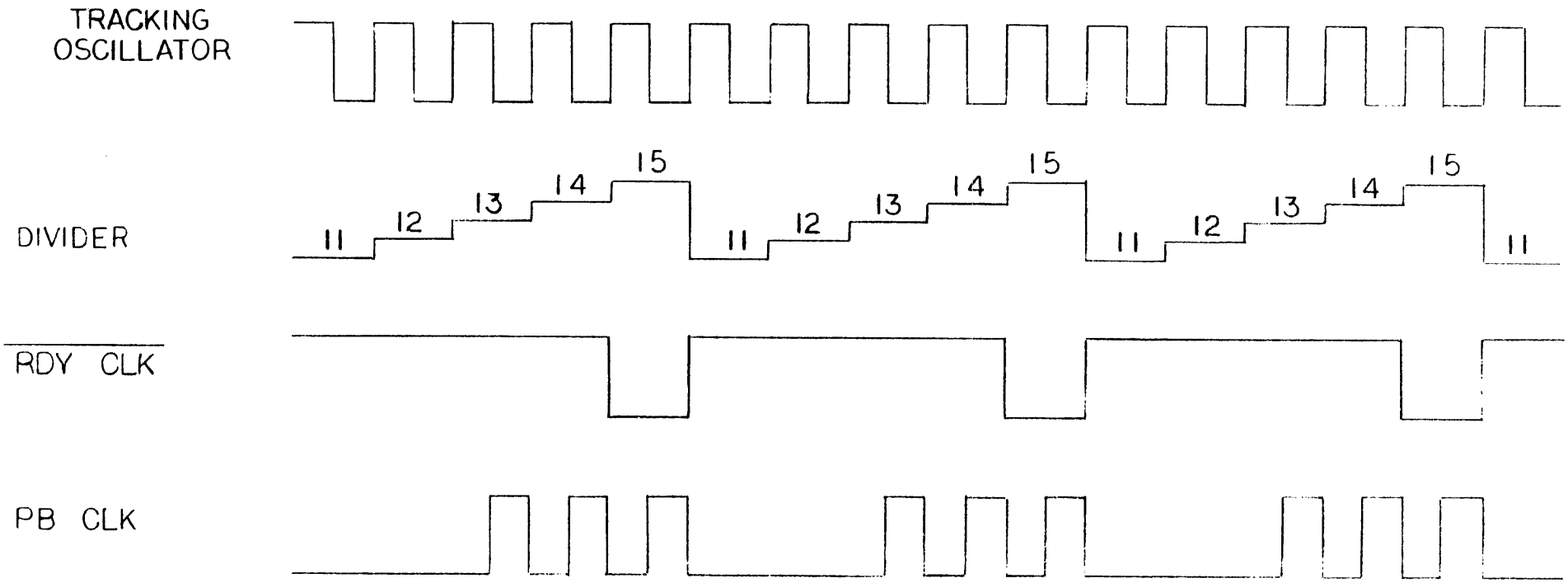


FIGURE 4-4 , PE READ TRACKING WAVEFORMS AT 45 IPS

encoded read decoding and deskewing logic (sheets 6-9); it occurs 70½ times per character period. See figures 4-3 and 4-4.

The tracking oscillator frequency varies with the tape speed and increases or decreases to maintain proper sampling rate. Before the ENB.DEC bit is set by the program the oscillator is held at center frequency. SYNCCLK3 indicates that a data transition has occurred in group 3. EARLY GATE (true when 24 or more RDYCLKS occur between data transitions) is sampled by the leading edge of RDYCLK. If EARLY GATE is false the frequency increases; if, on the other hand, EARLY GATE is true the frequency decreases. After reading the entire record ENB.DEC is cleared and the oscillator reverts to center frequency. This tracking is normally based on channel 2 (leading edge of RDY CLK); if channel 2 goes inactive the trailing edge of RDYCLK is used instead, thus sampling EARLY GATE in channel 1.

4.9.2 PE READ DECODING. The PE read decoding circuits distinguish the data portion of the record from the preamble and postamble and the data transition from the phase transition.

The nine read channels are multiplexed into three groups of three in the read input circuit (sheet 4). Each read input latch is loaded from the transport read data lines by RDCLK (inversion of PBCLK) when PBLOAD is high. PBLOAD is derived from RDYCLK and therefore occurs 23½ times per character period. The RDCLKs which are not enveloped by PBLOAD cause left-shifts. For example, at the cascade output of DECGRP1, channel 7 first appears, then channel 6, then channel 5, then channel 7 again and so forth. The sequence is load, shift, shift; load, shift, shift; etc. Note that RDNRZ false (high) prevents the outputs from going directly onto the D-bus. The decoding PROMs detect transitions by comparing inputs A_6 and A_7. If they are different a transition has occurred in that channel. (A_7 is the new level and A_6 is the old level.) PROM inputs A_0 - A_4 and outputs D_0-D_4 are used as a counter. This counter is restarted at 0 whenever a transition is detected, blocking the detection of further transitions until a count of 18 is reached and thus "hiding" the phase transition. Initially this circuit can detect only Ø transitions; synchronization in the preamble is therefore based upon the data transition. Each decoding circuit produces the following four time-multiplexed signals:

1) SYNCCLK: This signal is true after a data transition is decoded in the decoding PROM.

2) CLK: This signal is SYNCCLK after the end of the preamble is detected. The preamble "one" bit sets the ACTIVE latch, gating SYNCCLK to form CLK. CLK enters new data into the deskewing circuit.

3) DATA: This signal is true only when CLK is true and indicates that either a one or zero has been read in that channel.

4) INACTIVE: This signal indicates the absence of transitions in the channel being decoded or, after C ENB.SYNC, the loss of a transition.

EARLY GATE is true when 24 or more PBCLKs are required in a particular channel between data transitions. If the count should ever reach 31 after C ENB.SYNC is true, the channel's count locks up at 31, INACTIVE becomes

true, and no further transitions are detected for that channel until C ENB.SYNC is made false.

4.9.3 PE READ DESKEWING. The phase encoded read deskewing circuit consists of two 256 x 4 PROMs and three hex D-latches for each group of three multiplexed channels (sheets 6, 7, and 8). The first PROM directs incoming data (DATA when CLK is true) into one of four layers in the deskewing latches and recirculates any existing data.

The second PROM keeps track of the location of data in the deskewing register. A count which specifies the next empty layer is circulated in synchronization with the data. This PROM also generates two signals required by the common PE read circuits (sheet 9). OVFLOW indicates that all layers in the deskew register for that channel are full. OVFLOW in any channel produces the error signal DSKB FULL (Deskew Buffer Full). The second signal BITRDY, indicates that a bit is ready to be output. When BITRDY is true for all three groups for three consecutive PBCLKs, an entire phase encoded character is ready for output.

4.9.4 PE READ OUTPUT AND ERROR CORRECTION. When PECHRDY occurs three OUTCLKs transfer the "ready character" from the proper layer of the deskewing circuits into the output latches. The multiplexer selects the layer specified by the "read counter." Zero is transferred for any "inactive" channel.

Now the PBCHRDY flag is set. When PBCHRDY is serviced by the program the contents of the output latches are placed on the D-bus by the output PROM.

The "inactive latches" specify which if any of the channels are empty. When a PE character is moved from the data latches to the D-bus, the PE parity bit is inserted in any channel that is inactive. If more than one channel is inactive, however, the microprocessor halts further activity.

Postamble detection is relatively simple. When an "all ones" character is output on the Y-bus the ALL1OUT latch is set (sheet 2). If this is immediately followed by an "all zeroes" character the signal DETPP goes true to produce PPDET, which is tested by the program every character period.

The output and error correction PROM is also used by the program to determine activity in each channel. When searching for the beginning of a record the contents of the "inactive latches" are read to the D-bus. The D-bus is monitored by the D-bus monitor PROM which produces two signals, INACTIVE and INAMOD. Taken together, these signals reveal PE read activity.

CONDITION	INACTIVE	INAMOD
No channels inactive	False	False
One channel inactive	False	True
Two thru eight channels inactive	True	True
All channels inactive	True	False

The program sets the bit RQPESTS (request PE status) when looking for the beginning of a preamble. During this time only the condition of the "inactive latches" is gated onto the D-bus. The two flags, INACTIVE and INAMOD, are then tested often in the program. Eight channels must be active for fifteen consecutive character periods followed by four character periods without detecting a "one" to recognize a valid preamble.

A file mark is decoded if channels 2, 6, and 7 are "active" and channels 1, 3, and 4 are "inactive"; channels P, Ø, and 5 may each be either "active" or "inactive" in a file mark.

4.10 FORMATTER POWER SUPPLY. The formatter power supply is attached to the rear of the host transport's front plate. This power supply is a +5 VDC regulator with a maximum 10A output based on the transport's raw +8 VDC supply. Both foldback current limiting and overvoltage protection are provided. See schematic 0251536-0000 during the following circuit description.

Differential amplifier U1-3 compares the +5V output with a reference voltage established by adjusting potentiometer R28. The output of the differential amplifier drives emitter follower Q7, which provides base current to the five series-pass transistors Q1-Q5.

Foldback current is limited by the circuit centered upon U1-10 and U1-12. The first stage amplifies by approximately 26 the IR drop across power resistors R9-R13. The second stage compares this signal with the output voltage to select a maximum current value. As long as U1-14 is less positive than U1-13 CR2 is reverse biased. When, however, pin 14 rises to pin 13, CR2 will conduct, diverting current away from the base of Q7 to U1-12. This circuit limits current to 10A at +5V and to 3A with the output shorted.

Silicon-controlled rectifier Q6 provides overvoltage protection. When the output voltage exceeds 6.3 volts Q8 turns on, firing Q6 and blowing fuse F1.

9 TRACK	12.5	18.75	25	37.5	45	75
WRT/RD FROM BOT	87.5	58.3	43.8	29.2	24.3	14.6
WRITE NORMAL	33.2	22.1	16.6	11.1	9.24	5.54
READ NORMAL	30.1	20.0	15.0	10.0	8.35	5.01
FIRST WRITE CLOCK						
SINGLE GAP	18.8	12.5	9.41	6.27	5.23	3.14
DUAL GAP	6.82	4.54	3.41	2.27	1.89	1.14
POST RECORD DELAY						
WRITE SINGLE GAP	22.1	14.7	11.1	7.37	6.14	3.68
WRITE DUAL GAP	22-22.4	14.6-14.9	11.0-11.2	7.33-7.46	6.11-6.22	3.67-3.73
READ FWD	4.01	2.67	2.00	1.34	1.11	.668
READ REV	3.47	2.31	1.74	1.15	.964	.578
READ REV EDIT	25.1	16.7	12.5	8.36	6.96	4.18
STAY AT SPD WINDOW	33.1	22.1	16.5	11.0	9.19	5.51
TRANSPORT STOPPING	33.1	22.1	16.5	11.0	9.20	5.52

7 TRACK	12.5	18.75	25	37.5	45	75
WRT/RD FROM BOT	87.5	58.3	43.8	29.2	24.3	14.6
WRITE NORMAL	33.2	22.1	16.6	11.1	9.24	5.54
READ NORMAL	30.1	20.0	15.0	10.0	8.35	5.01
FIRST WRITE CLOCK						
SINGLE GAP	30.8	20.5	15.4	10.3	8.56	5.14
DUAL GAP	6.82	4.54	3.41	2.27	1.89	1.14
POST RECORD DELAY						
WRITE SINGLE GAP	33.7	22.5	16.8	11.2	9.36	5.62
WRITE DUAL GAP	21.7-22	14.5-14.7	10.9-11.0	7.25-7.33	6.04-6.11	3.62-3.67
READ FWD	3.73	2.48	1.86	1.24	1.04	.621
READ REV	15.5	10.3	7.74	5.16	4.30	2.58
READ REV EDIT	37.1	24.7	18.5	12.4	10.3	6.18
STAY AT SPD WINDOW	33.1	22.1	16.5	11.0	9.19	5.51
TRANSPORT STOPPING	33.1	22.1	16.5	11.0	9.20	5.52

All times are given in milliseconds.

Figure 4-5, Formatter Timing

5 - MAINTENANCE

5.1 FAULT ISOLATION. The following procedure for fault isolation allows the maintenance engineer to determine whether or not a system malfunction is caused by the formatter.

1) Connect a voltmeter between the formatter's power connections. Verify that the meter indicates +5V ± 0.25. Refer to paragraph 5.4.1 regarding power supply adjustment, and to paragraph 5.2 regarding power supply replacement, as necessary.

2) Disconnect all daisy-chained transports. Move the termination packs from the last transport's write/control card to the write/control card of the transport housing the formatter. Disconnect the controller cables and connect a Digi-Data test card to the formatter/controller I/O. To supply power to the test card move the formatter plug jumper WD to WC. Operate the test card in the "write check" mode. (Note: If a Digi-Data test card is not available the Digi-Data hardware diagnostics for the NOVA, PDP-11, or HP2100 tape system may be used with a known good interface.) Does the system work now? In both NRZ and PE (if applicable)? If so, one of the disconnected transports is suspect.

3) If the system continues to fail, attempt to write with formatter ".SGL" (sheet 1) grounded (disabling the read-after-write) to determine if the problem is in the write or read circuits or common to both. Also monitor the output signals from the formatter to the transport's write/control card. Insure that all lines (e.g. SFC, SWS, etc.) toggle or are at the proper levels.

4) If all lines appear correct troubleshoot the transport; otherwise, replace the formatter card. See paragraph 5.3.

5.2 FORMATTER POWER SUPPLY REPLACEMENT. The +5 VDC power supply for the embedded formatter is mounted on the rear of the transport front plate. To remove and replace this unit perform the following sequence.

1) Pull off the six quick-disconnect wires which connect the power supply to the transport and to the formatter.

2) Remove the two screws which hold the power supply assembly to the plate and remove the assembly; see drawing 0052701-0000.

3) Apply thermal compound to the replacement assembly's mounting surface and to the mounting surface of the plate. Mount the assembly with two screws and washers.

4) Push on the six electrical connections. Refer to assembly drawing 0051533-0000.

E1	(black)	formatter ground post
E2	(black)	C2 (-), ground
E3	(red)	formatter +5V post
E4	(red)	C2 (+), raw +8V
E5	(green)	JA-N, 12V
E6	(orange)	JB-6, +12V

5) See paragraph 5.4.1 to adjust the +5 VDC output.

5.3 FORMATTER CARD REPLACEMENT. To remove and replace the formatter card perform the following steps.

1) Unplug the controller and transport connectors.

2) Remove the black and red power connections.

3) Remove the screws which hold the card to the card cage, and remove the card; see drawing 0052701-0000, Installation Drawing Formatter Kit, located at the end of this manual.

4) Mount the replacement card with hardware. Check that all plug jumpers on the replacement card are in the desired position. Refer to paragraph 1.5. Also check that the termination packs are installed; see figure 2-6.

5) Reconnect the red and black power supply wires to the formatter card.

6) Plug in the I/O cables at top and bottom.

5.4 FORMATTER ADJUSTMENTS.

5.4.1 POWER SUPPLY ADJUSTMENT. Connect a voltmeter across the power posts on the formatter card. Adjust potentiometer R28 in the front plate-mounted power assembly to read +5.0 ±0.25 volts. If the power supply cannot be adjusted to +5.0 volts remove the red wire to isolate the supply from its load. Also check the +8 volt input to this regulator at the terminals of filter capacitor C2. See schematic 0251536-0000 located at the end of this manual. Replace the power supply assembly or formatter assembly as necessary.

5.4.2 ADJUSTMENT OF THE PHASE ENCODED READ TRACKING OSCILLATORS. Read any tape written in blocks at 1600 BPI. A transport operating at 75, 45, or 25 IPS uses the PE read tracking ocillator #1; a transport operating at 37.5, 18.75, or 12.5 IPS uses oscillator #2.

Connect an oscilloscope to Pin 1 of oscillator U10B and adjust potentiometers so that the center voltage approximates the tracking voltage. See Figure 5-1. The transport speed control switches must be changed to select the second potentiometer.

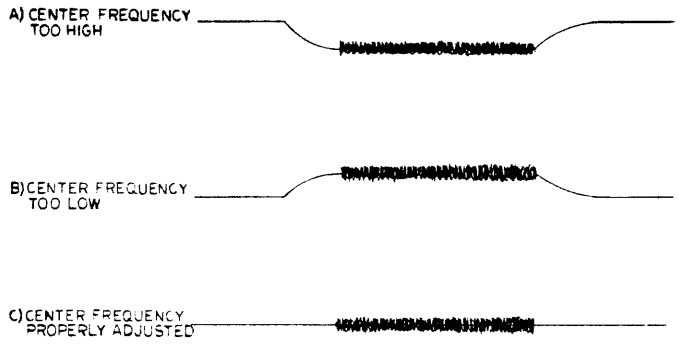


FIGURE 5-1, ADJUSTMENT OF THE READ TRACKING OSCILLATORS

ENGINEERING DOCUMENTATION

SCHEMATICS

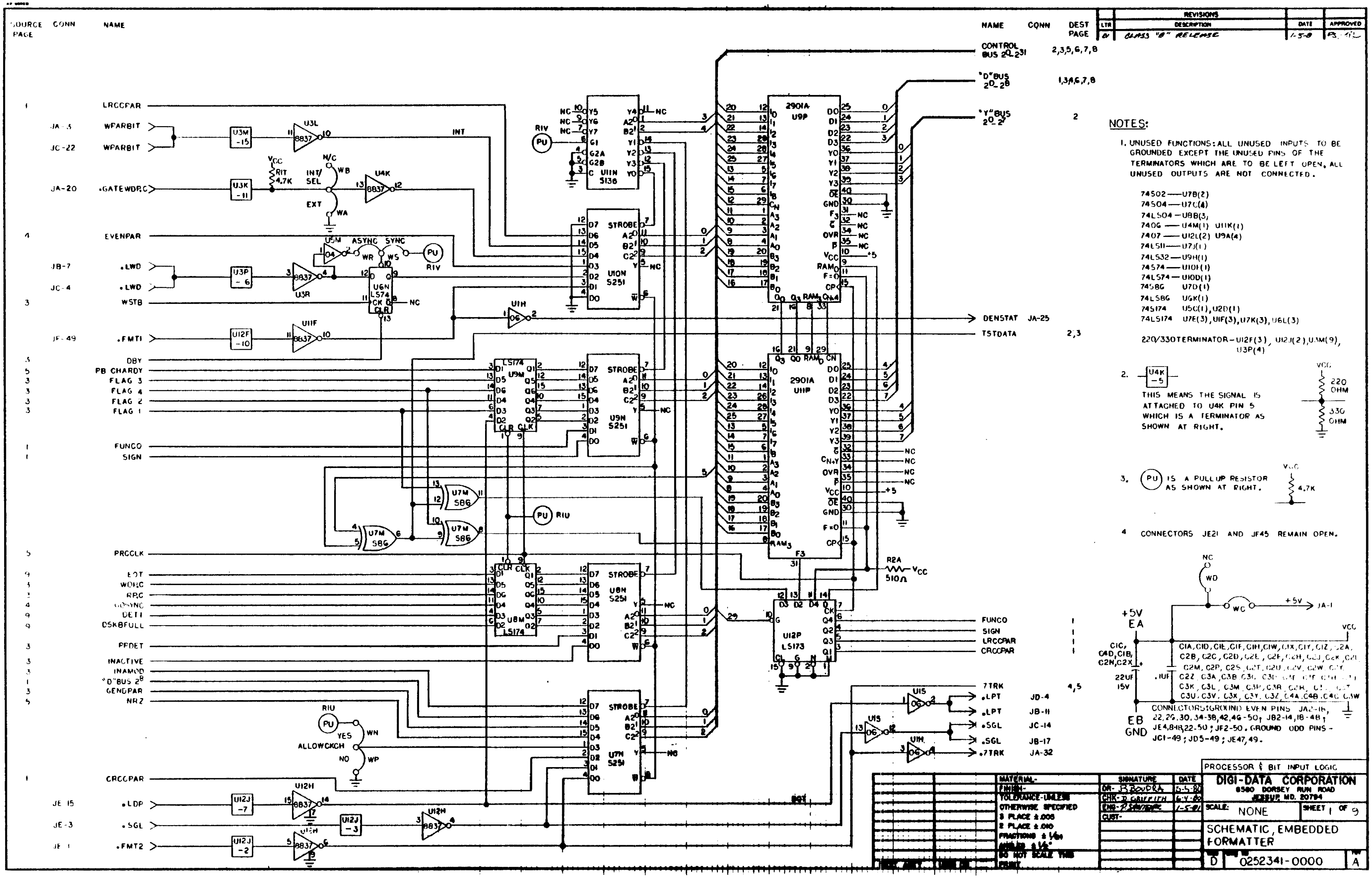
Schematic, Embedded Formatter	0252341-0000
Schematic, Formatter Power Supply	0251536-0000

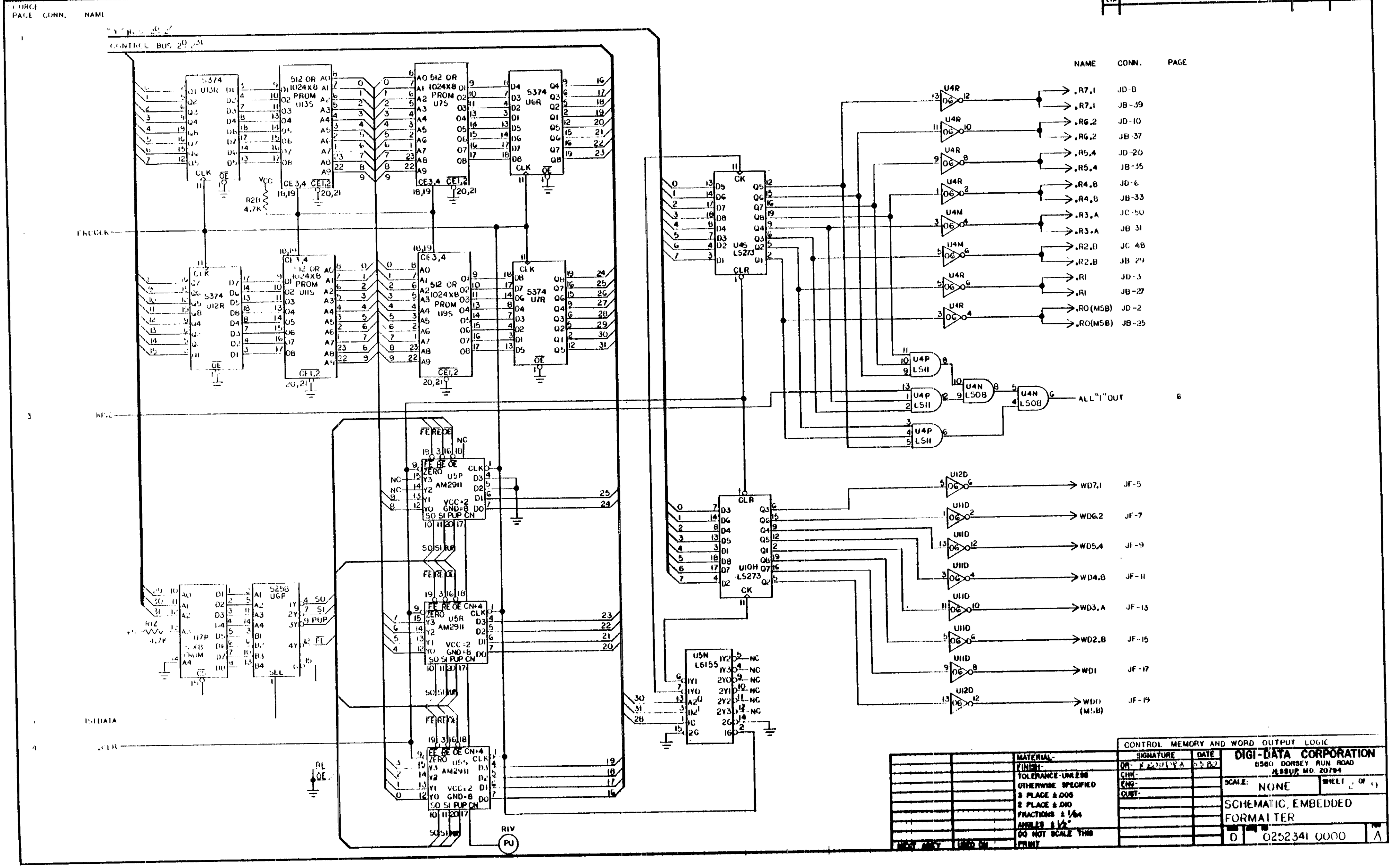
ASSEMBLY DRAWINGS

Assembly, Embedded Formatter	0052645-0000
Assembly, Formatter Power Supply	0051533-0000
Installation Drawing Formatter Kit	0052701-0000
Kit, Cable, Embedded Formatter to Transport	0052160-0000
Kit, Formatter Terminator	0052702-0000

ASSEMBLY PARTS LISTS

Assembly, Embedded Formatter, P/L	0052645-0001 thru -0002
Assembly, Formatter Power Supply P/L	0051533-0001
Embedded Formatter, Kit; P/L	0052701-0001 thru -0003
Kit, Cable, Embedded Formatter to Transport, P/L	0052160-0001 thru -0004
Kit, Formatter Terminator, P/L	0052702-0001


SOURCE PAGE
CONN
NAME
DEST PAGE
REVISIONS
LTR
DESCRIPTION
DATE
APPROVED
A CLASS "B" RELEASE
CONTROL BUS 2^0-2^31
"D" BUS 2^0-2^8
"Y" BUS 2^0-2^7
NOTES:
1. UNUSED FUNCTIONS: ALL UNUSED INPUTS TO BE GROUNDED EXCEPT THE UNUSED PINS OF THE TERMINATORS WHICH ARE TO BE LEFT OPEN. ALL UNUSED OUTPUTS ARE NOT CONNECTED.
74S02 — U7B(2)
74S04 — U7C(4)
74LS04 — U8B([illegible])
7406 — U4M(1) U11K(1)
7407 — U12L(2) U9A(4)
74LS11 — U7J(1)
74LS32 — U9H(1)
74S74 — U10F(1)
74LS74 — U10D(1)
74S86 U7D(1)
74LS86 U6K(1)
74S174 U5C(1), U2D(1)
74LS174 U7E(3), U1F(3), U7K(3), U6L(3)
220/330 TERMINATOR — U12F(3), U12J(2), U3M(9), U3P(4)
2. THIS MEANS THE SIGNAL IS ATTACHED TO U4K PIN 5 WHICH IS A TERMINATOR AS SHOWN AT RIGHT.
3. (PU) IS A PULLUP RESISTOR AS SHOWN AT RIGHT.
4 CONNECTORS JE21 AND JF45 REMAIN OPEN.
PROCESSOR & BIT INPUT LOGIC
DIGI-DATA CORPORATION
8580 DORSEY RUN ROAD
JESSUP, MD. 20794
SCALE: NONE
SHEET 1 OF 9
SCHEMATIC, EMBEDDED FORMATTER
D 0252341-0000 A
MATERIAL-
FINISH-
TOLERANCE-UNLESS OTHERWISE SPECIFIED
3 PLACE ±.005
2 PLACE ±.010
FRACTIONS ± 1/64
ANGLES ± 1/2°
DO NOT SCALE THIS PRINT



CONTROL MEMORY AND WORD OUTPUT LOGIC

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

MATERIAL-
FINISH-
TOLERANCE-UNLESS OTHERWISE SPECIFIED
3 PLACE ±.005
2 PLACE ±.010
FRACTIONS ± 1/64
ANGLES ± 1/2°
DO NOT SCALE THIS PRINT

NEXT ASSY | USED ON

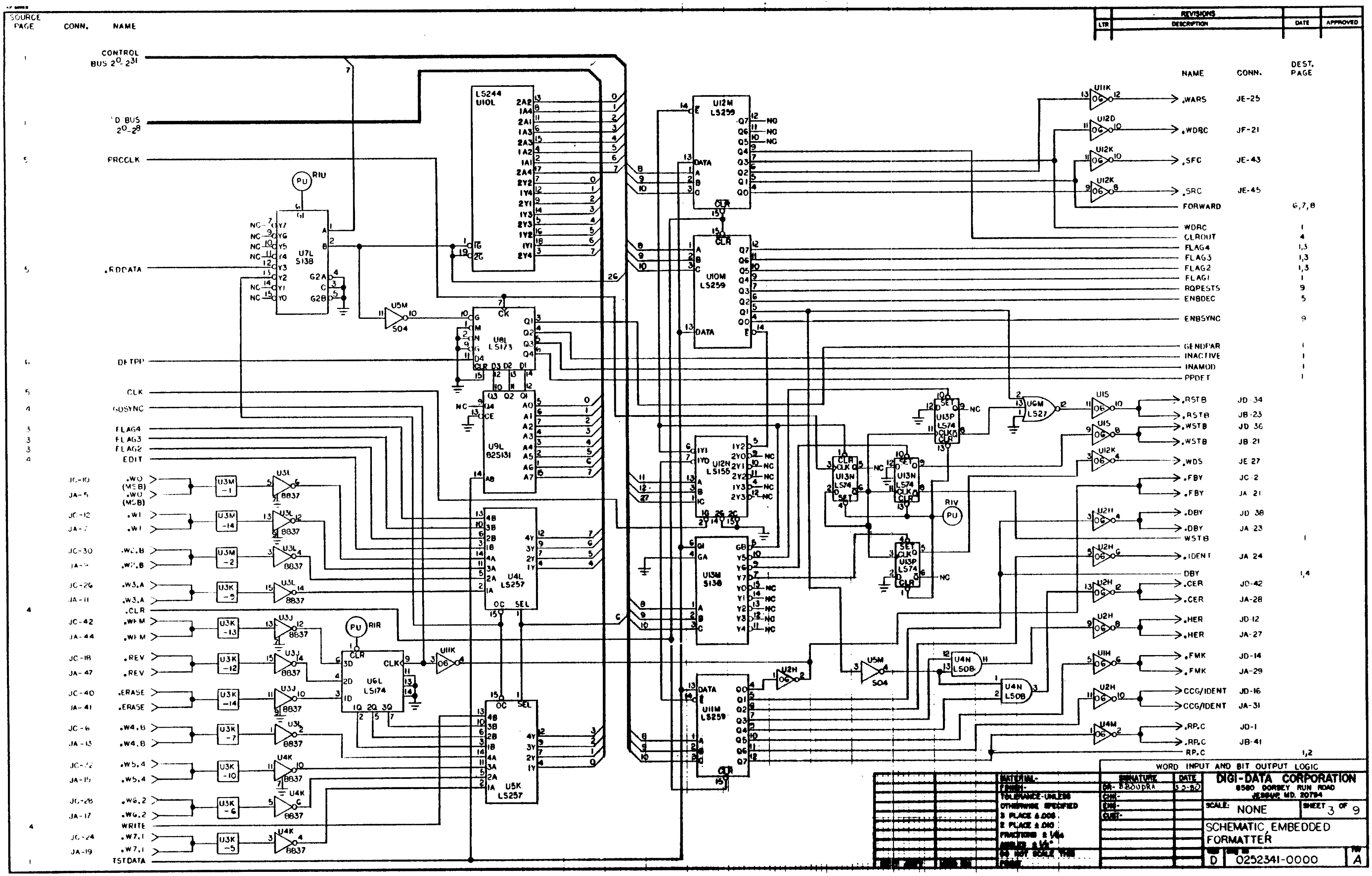
SIGNATURE | DATE
DR- | 5-5-82
CHK-
ENG-
CUST-

DIGI-DATA CORPORATION
8580 DORSEY RUN ROAD
JESSUP MD. 20794

SCALE: NONE
SHEET 2 OF 9

SCHEMATIC, EMBEDDED FORMATTER

SIZE D | DWG NO 0252341 0000 | REV A



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D BUS 2^0-2^8
FRCCLK
.RDDATA
DETPP
CLK
GOSYNC
FLAG4
FLAG3
FLAG2
EDIT
.CLR
WRITE
TSTDATA
NAME
CONN.
DEST. PAGE
.WARS
.WDRC
.SFC
.SRC
FORWARD
WDRC
CLROUT
FLAG4
FLAG3
FLAG2
FLAG1
RQPESTS
ENBDEC
ENBSYNC
GENDPAR
INACTIVE
INAMOD
PPDET
.RSTB
.WSTB
.WDS
.FBY
.DBY
WSTB
.IDENT
DBY
.CER
.HER
.FMK
CCG/IDENT
.RP.C
RP.C
REVISIONS
LTR
DESCRIPTION
DATE
APPROVED
WORD INPUT AND BIT OUTPUT LOGIC
DIGI-DATA CORPORATION
8580 DORSEY RUN ROAD
JESSUP, MD. 20794
SCALE: NONE
SHEET 3 OF 9
SCHEMATIC, EMBEDDED FORMATTER
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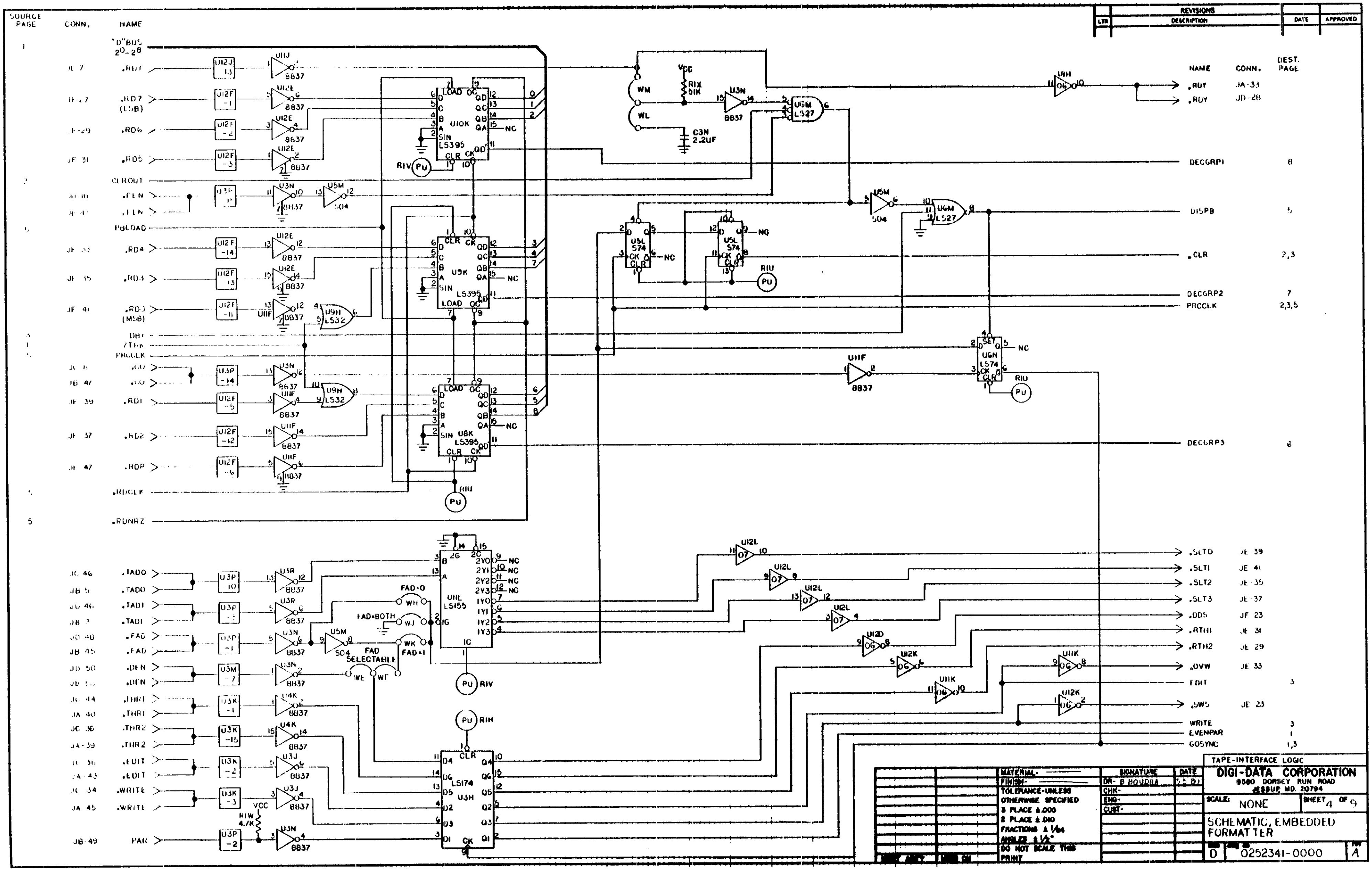

SOURCE PAGE
CONN.
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.RD7 (LSB)
.RD6
.RD5
CLROUT
.FEN
PBLOAD
.RD4
.RD3
.RD0 (MSB)
PRCCLK
.RD1
.RD2
.RDP
.RDCLK
.RDNRZ
.TAD0
.TAD1
.FAD
.DEN
.THR1
.THR2
.EDIT
.WRITE
PAR
U10K LS395
U9K LS395
U8K LS395
U11L LS155
U3H LS174
U5L S74
U6N LS74
FAD=0
FAD=BOTH
FAD=1
FAD SELECTABLE
REVISIONS
LTR
DESCRIPTION
DATE
APPROVED
NAME
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.RDY JD-28
DECGRP1 8
DISPB 5
.CLR 2,3
DECGRP2 7
PRCCLK 2,3,5
DECGRP3 6
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.SLT1 JE 41
.SLT2 JE 35
.SLT3 JE 37
.DDS JF 23
.RTH1 JE 31
.RTH2 JE 29
.OVW JE 33
EDIT 3
.SW5 JE 23
WRITE 3
EVENPAR 1
GOSYNC 1,3
TAPE-INTERFACE LOGIC
DIGI-DATA CORPORATION
8580 DORSEY RUN ROAD
JESSUP, MD. 20794
MATERIAL-
FINISH-
TOLERANCE-UNLESS OTHERWISE SPECIFIED
3 PLACE ±.005
2 PLACE ±.010
FRACTIONS ± 1/64
ANGLES ± 1/2°
DO NOT SCALE THIS PRINT
SIGNATURE
DATE
DR- B HOUDRA
CHK-
ENG-
CUST-
SCALE: NONE
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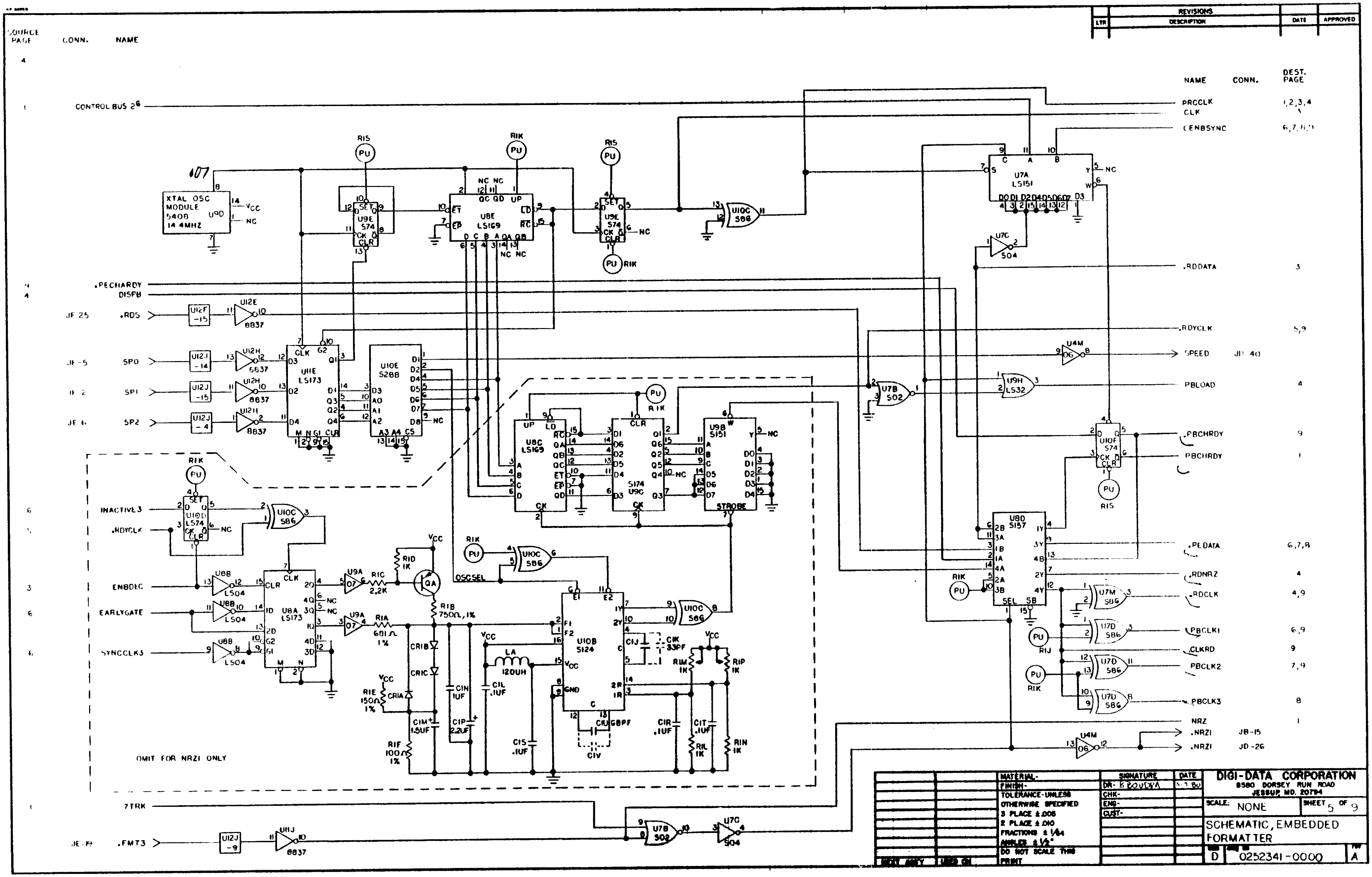
D
0252341-0000
A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DISPB
.RDS
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SP1
SP2
INACTIVE3
.RDYCLK
ENBDEC
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SYNCCLK3
OMIT FOR NRZI ONLY
7TRK
.FMT3
XTAL OSC MODULE 5408 14.4MHZ
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DEST. PAGE
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CLK
CENBSYNC
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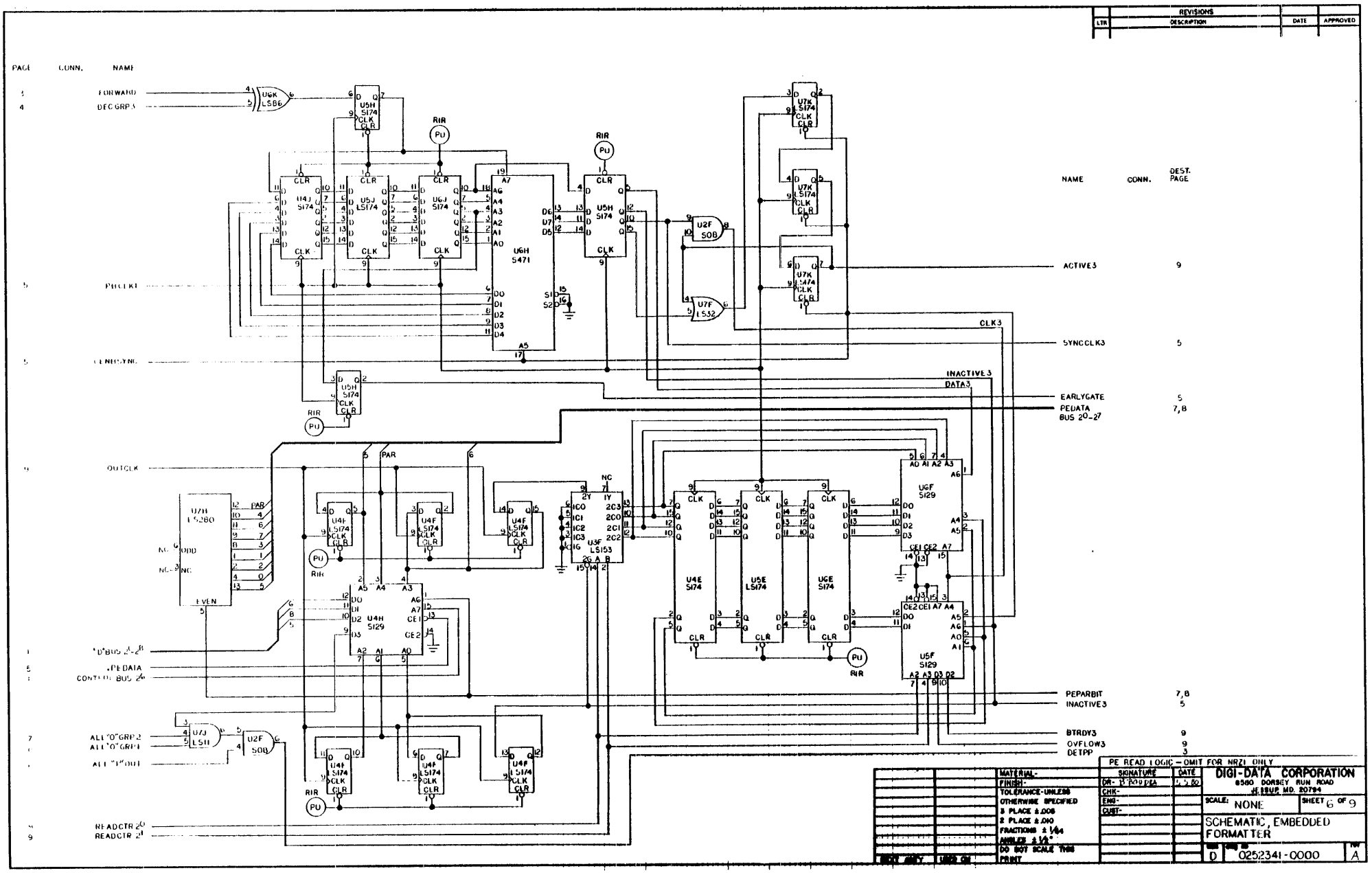
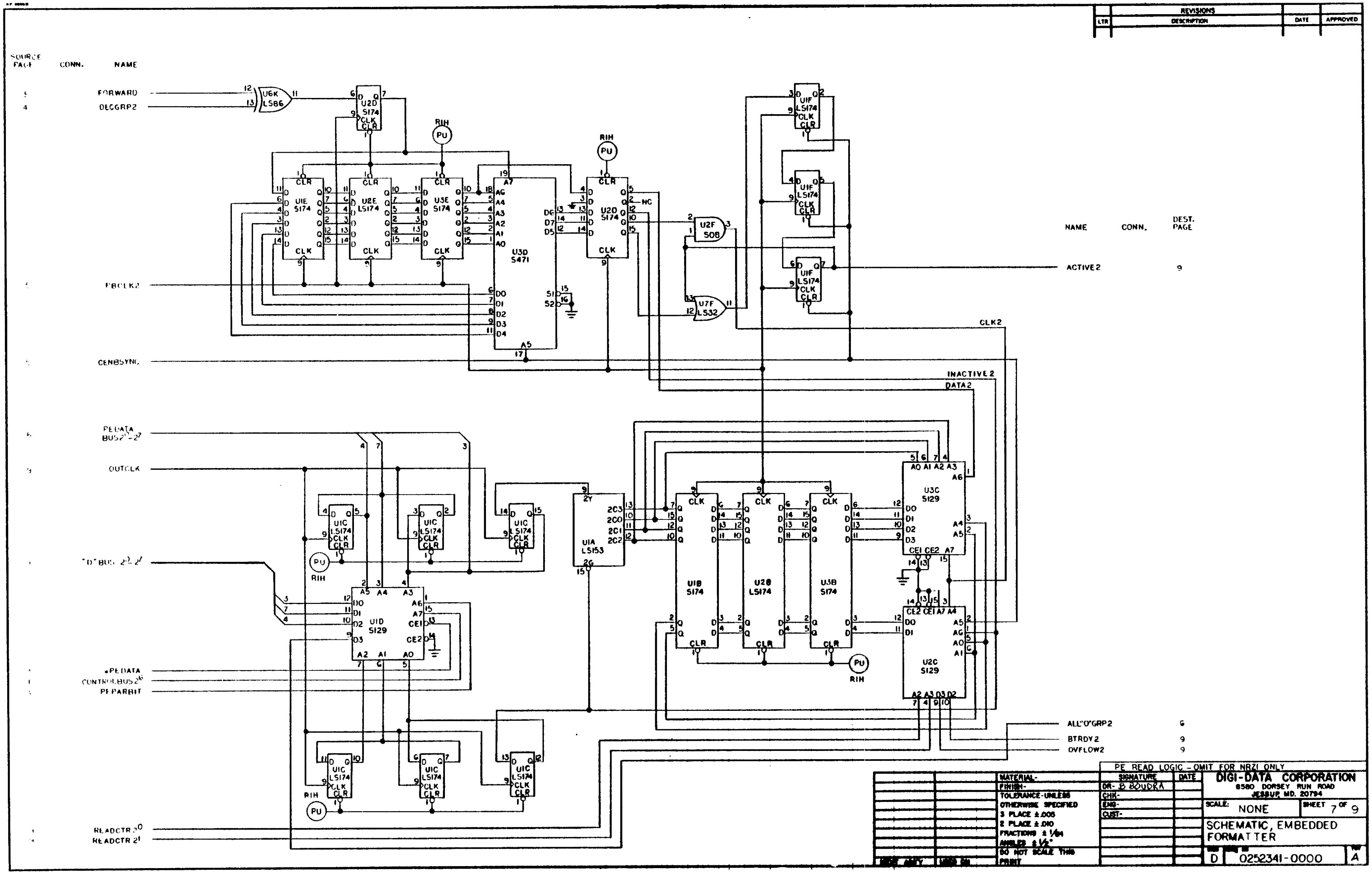
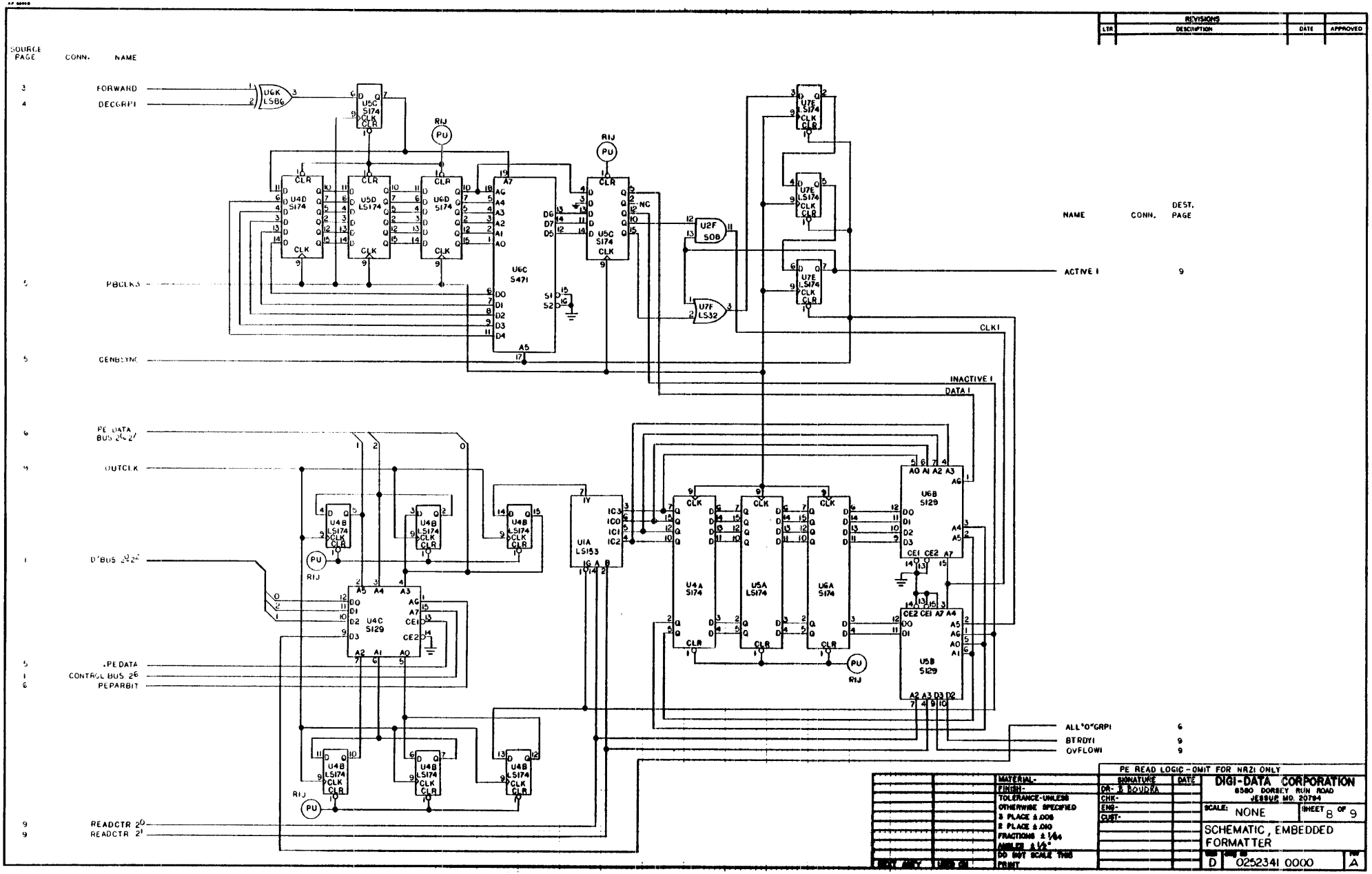
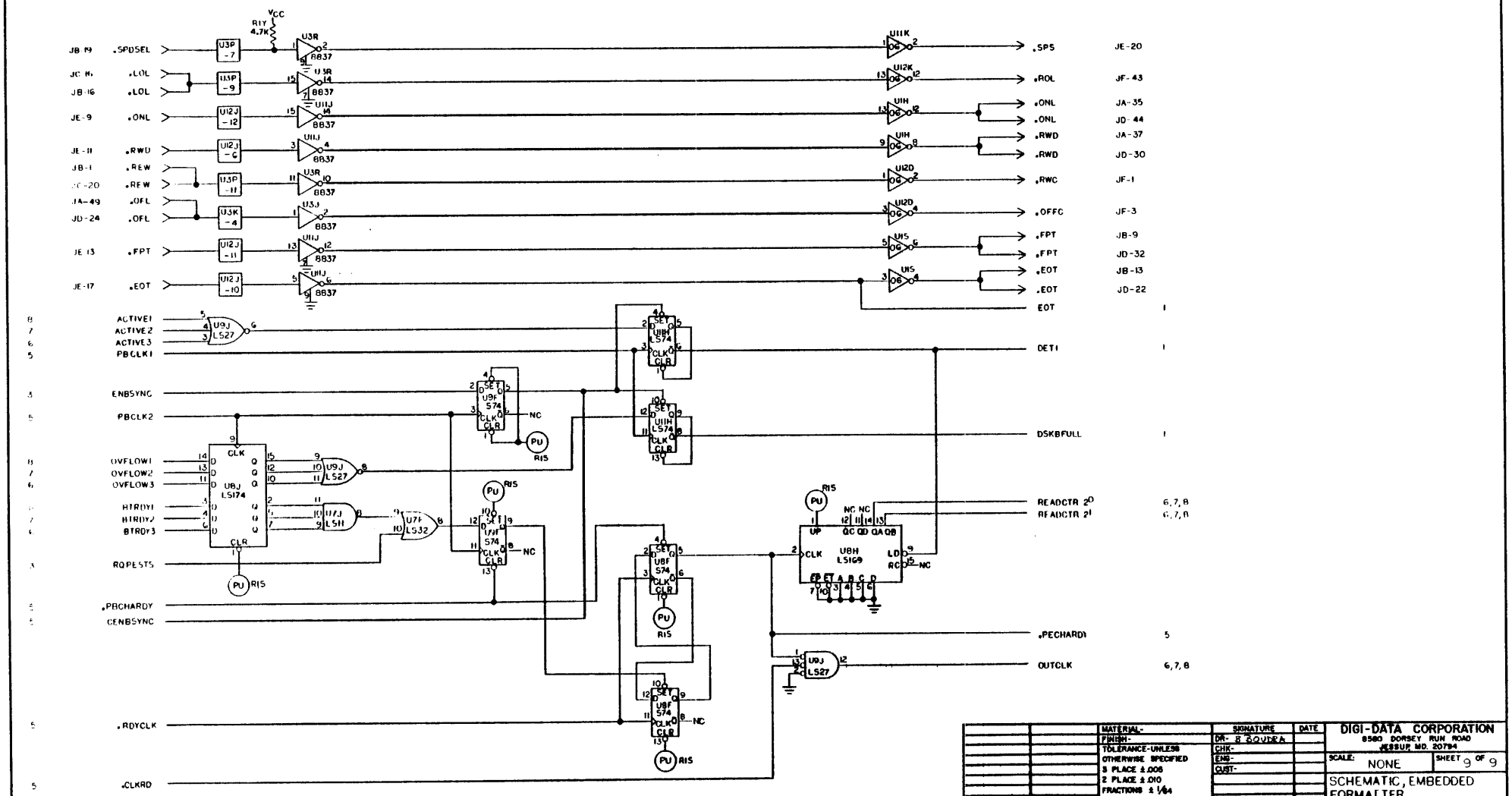
.RDYCLK
SPEED
PBLOAD
.PBCHRDY
PBCHRDY
.PEDATA
.RDNRZ
.RDCLK
.PBCLK1
CLKRD
PBCLK2
.PBCLK3
NRZ
.NRZI
.NRZI
REVISIONS
LTR
DESCRIPTION
DATE
APPROVED
MATERIAL-
FINISH-
TOLERANCE-UNLESS OTHERWISE SPECIFIED
3 PLACE ±.005
2 PLACE ±.010
FRACTIONS ±1/64
ANGLES ±1/2°
DO NOT SCALE THIS PRINT
NEXT ASSY
USED ON
SIGNATURE
DATE
DR-
CHK-
ENG-
CUST-
DIGI-DATA CORPORATION
8580 DORSEY RUN ROAD
JESSUP, MD. 20794
SCALE: NONE
SHEET 5 OF 9
SCHEMATIC, EMBEDDED FORMATTER
D
0252341-0000
A


REVISIONS
LTR
DESCRIPTION
DATE
APPROVED
PAGE
CONN.
NAME
FORWARD
DECGRP3
PBCLKT
CENSYNC
OUTCLK
"D"BUS 20-28
PEDATA
CONTROL BUS 20
ALL "0"GRP2
ALL "0"GRP1
ALL "1"OUT
READCTR 20
READCTR 21
PAR
RIR
PU
NAME
CONN.
DEST. PAGE
ACTIVE3
9
CLK3
SYNCCLK3
5
INACTIVE3
DATA3
EARLYGATE
5
PEDATA BUS 20-27
7,8
PEPARBIT
7,8
INACTIVE3
5
BTRDY3
9
OVFLOW3
9
DETPP
3
PE READ LOGIC - OMIT FOR NRZI ONLY
MATERIAL-
FINISH-
TOLERANCE-UNLESS OTHERWISE SPECIFIED
3 PLACE ± .005
2 PLACE ± .010
FRACTIONS ± 1/64
ANGLES ± 1/2°
DO NOT SCALE THIS PRINT
SIGNATURE
DATE
DR-
CHK-
ENG-
CUST-
DIGI-DATA CORPORATION
8580 DORSEY RUN ROAD
JESSUP, MD. 20794
SCALE: NONE
SHEET 6 OF 9
SCHEMATIC, EMBEDDED FORMATTER
SIZE
D
025234 1-0000
REV
A


REVISIONS
LTR
DESCRIPTION
DATE
APPROVED
SOURCE PAGE
CONN.
NAME
FORWARD
DECGRP2
PBCLK2
CENBSYNC
PEDATA BUS 2⁰-2⁷
OUTCLK
TD BUS 2⁰-2⁷
PEDATA
CONTROLBUS 2⁶
PEPARBIT
READCTR 2⁰
READCTR 2¹
U6K LS86
U2D S174
U1E S174
U2E LS174
U3E S174
U3D S471
U2D S174
U2F S08
U7F LS32
U1F LS174
RIH
PU
NAME
CONN.
DEST. PAGE
ACTIVE2
CLK2
INACTIVE2
DATA2
U1A LS153
U1B S174
U2B LS174
U3B S174
U3C S129
U2C S129
U1D S129
U1C LS174
ALL"O"GRP2
BTRDY2
OVFLOW2
PE READ LOGIC - OMIT FOR NRZI ONLY
MATERIAL-
FINISH-
TOLERANCE-UNLESS OTHERWISE SPECIFIED
3 PLACE ±.005
2 PLACE ±.010
FRACTIONS ± 1/64
ANGLES ± 1/2°
DO NOT SCALE THIS PRINT
NEXT ASSY
USED ON
SIGNATURE
DATE
DR- B BOUDRA
CHK-
ENG-
CUST-
DIGI-DATA CORPORATION
8580 DORSEY RUN ROAD
JESSUP, MD. 20794
SCALE: NONE
SHEET 7 OF 9
SCHEMATIC, EMBEDDED FORMATTER
D
0252341-0000
A

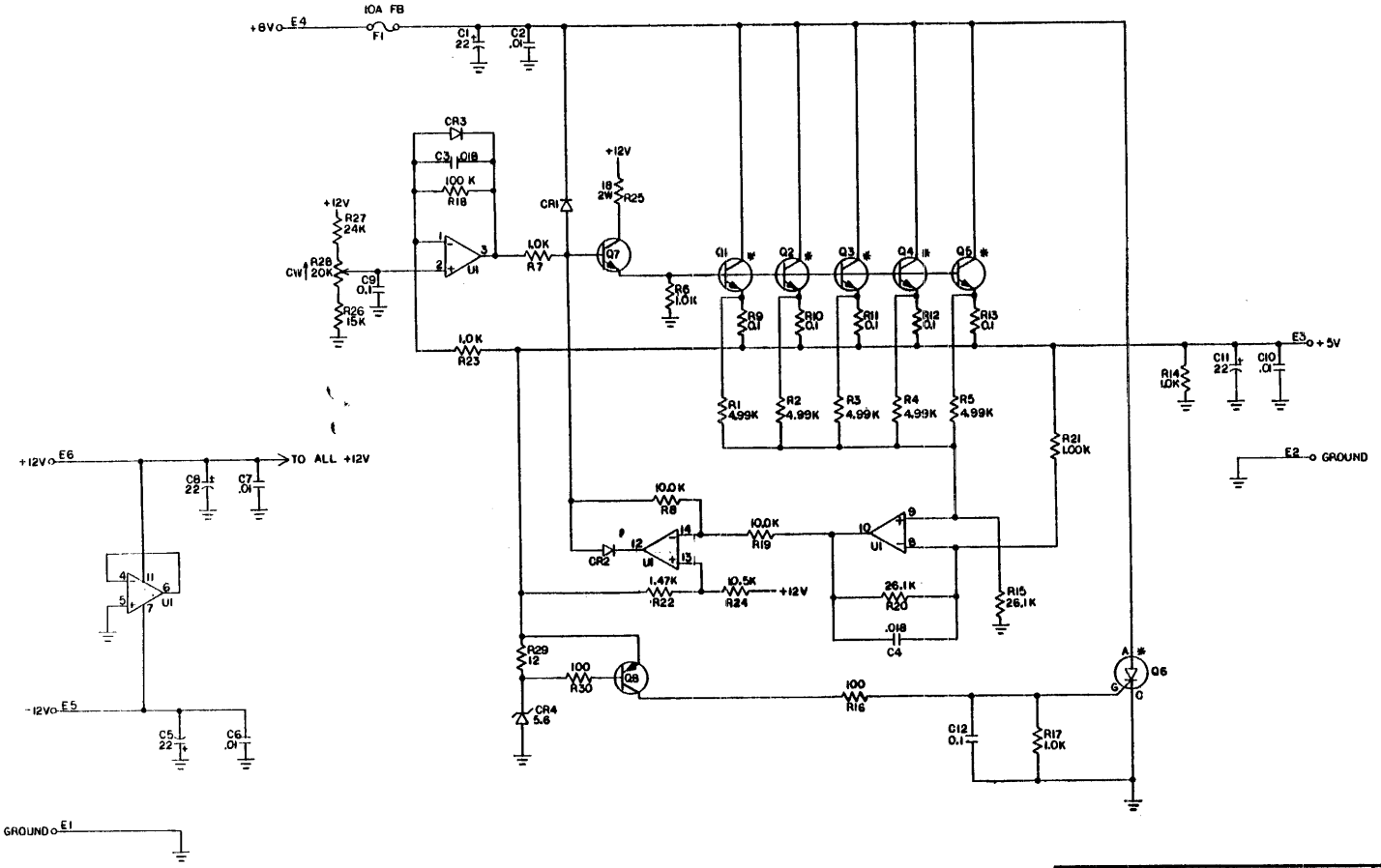

REVISIONS
LTR DESCRIPTION DATE APPROVED
SOURCE PAGE CONN. NAME
3 FORWARD
4 DECGRPI
5 PBCLKS
5 CENBSYNC
6 PE DATA BUS 2^6 2^7
9 OUTCLK
1 D'BUS 2^6 2^7
5 PE DATA
1 CONTROL BUS 2^6
6 PEPARBIT
9 READCTR 2^0
9 READCTR 2^1
NAME CONN. DEST. PAGE
ACTIVE I 9
CLK I
INACTIVE I
DATA I
ALL "0" GRPI 6
BTRDYI 9
OVFLOWI 9
U6K LS86
U5C S174
U4D S174
U5D LS174
U6D S174
U6C S471
U5C S174
U2F 508
U7F LS32
U7E LS174
U4B LS174
U4C S129
U1A LS153
U4A S174
U5A LS174
U6A S174
U6B S129
U5B S129
RIJ
PU
PE READ LOGIC - OMIT FOR NRZI ONLY
MATERIAL-
FINISH-
TOLERANCE-UNLESS OTHERWISE SPECIFIED
3 PLACE ± .005
2 PLACE ± .010
FRACTIONS ± 1/64
ANGLES ± 1/2°
DO NOT SCALE THIS PRINT
SIGNATURE DATE
DR- B BOUDRA
CHK-
ENG-
CUST-
DIGI-DATA CORPORATION
8580 DORSEY RUN ROAD
JESSUP MD. 20794
SCALE: NONE
SHEET 8 OF 9
SCHEMATIC, EMBEDDED FORMATTER
D 0252341 0000 A

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



		MATERIAL-	SIGNATURE	DATE	DIGI-DATA CORPORATION	
		FINISH-	DR- R GOUDEA		8580 DORSEY RUN ROAD	
		TOLERANCE-UNLESS	CHK-		JESSUP, MD. 20794	
		OTHERWISE SPECIFIED	ENG-		SCALE: NONE	SHEET 9 OF 9
		3 PLACE ±.005	CUST-		SCHEMATIC, EMBEDDED FORMATTER	
		2 PLACE ±.010				
		FRACTIONS ± 1/64			SIZE D	DWG NO 0252341-0000
		ANGLES ± 1/2°				REV A
NEXT ASSY	USED ON	DO NOT SCALE THIS PRINT				

LTR	REVISIONS DESCRIPTION	DATE	APPROVED
01	CLASS 'B' RELEASE	8-17-78	JTE

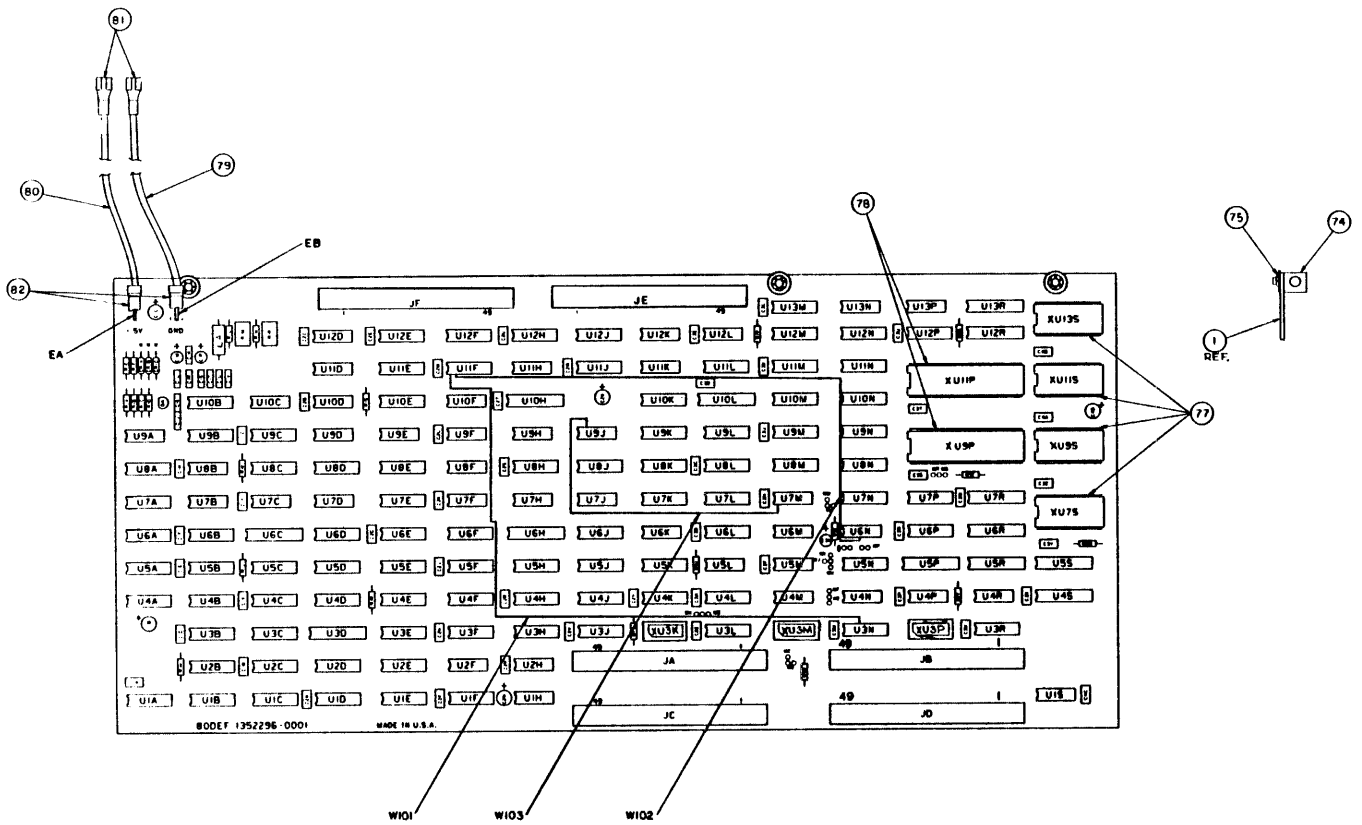


NOTES:
1. UNLESS OTHERWISE SPECIFIED
   A. ALL RESISTANCES ARE IN OHMS.
   B. ALL CAPACITANCES ARE IN MICROFARADS.
2 * = ON HEATSINK

	MATERIAL-	DR- S. HEISHMAN	7/25/78	DIGI-DATA CORPORATION 8580 DORSEY RUN ROAD JESSUP, MD. 20794
	FINISH-	CHK-	8-17-78	
	TOLERANCE-UNLESS OTHERWISE SPECIFIED 3 PLACE ± .005 2 PLACE ± .010 FRACTIONS ± 1/64 ANGLES ± 1/2° DO NOT SCALE THIS PRINT	ENG- JTE	8-17-78	SCALE: NONE SHEET 1 OF 1
		CUST-		SCHEMATIC, FORMATTER POWER SUPPLY
				SIZE D DWG NO 0251536-0000 REV 01

DDC PART NO.	APPLICABLE NOTES
0052645-0001	1,2,3,5,6
0052645-0002	1,2,3,4,5,6,7

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
01	CLASS "B" RELEASE		

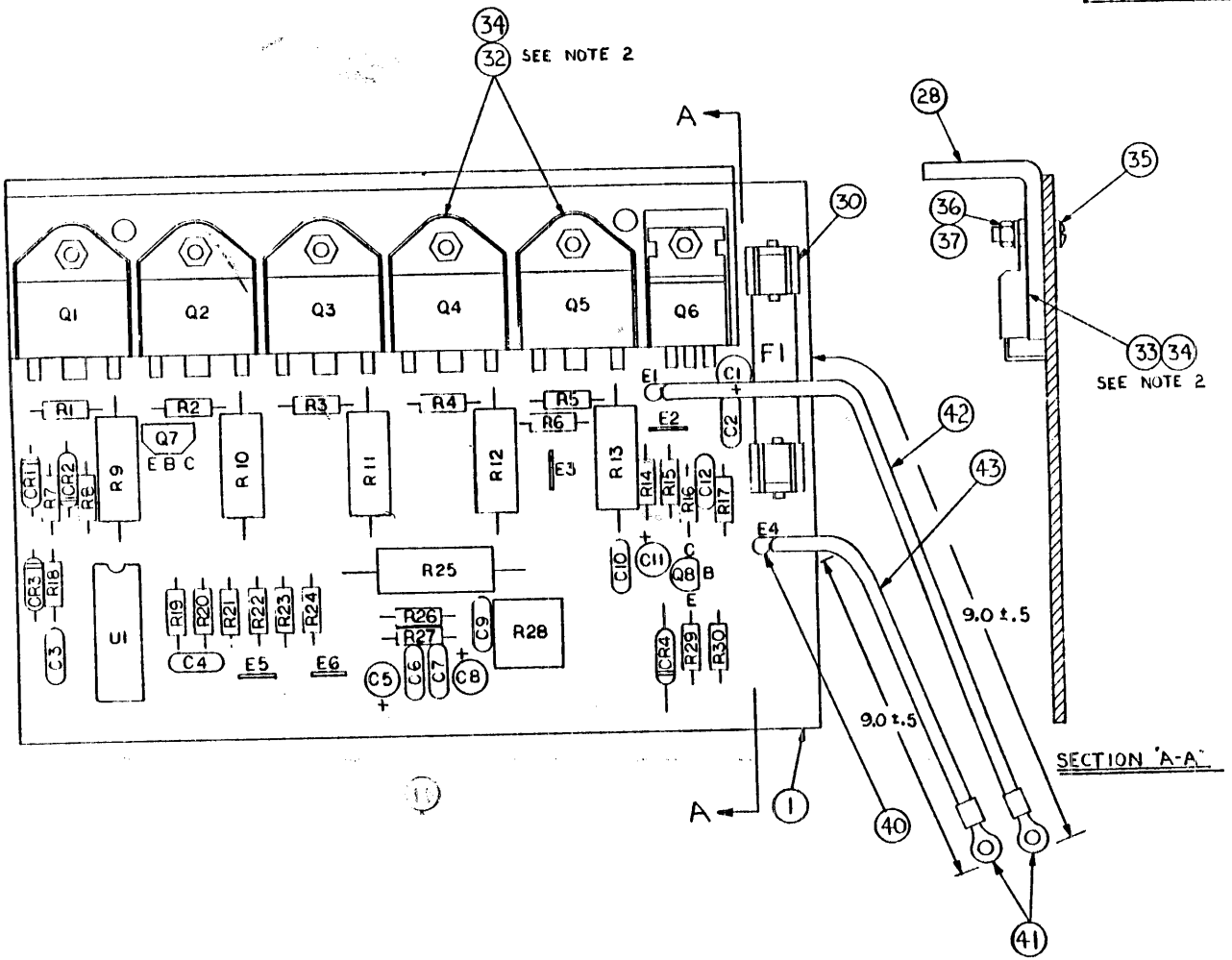


NOTES:

1. D.D.C. PART NUMBER AND LATEST REV LEVEL TO BE STAMPED ON COMPONENT SIDE OF BOARD.
2. CUT LAND RUNNING FROM U6N PIN 3 TO U3N PIN 12.
3. CUT LAND RUNNING FROM U11F PIN 1 TO U11F PIN 7.
4. CUT LAND RUNNING FROM U9J PIN 13 TO U10K PIN 10.
5. ADD WIRE JUMPER W101 FROM U11F PIN 1 TO U3N PIN 12.
6. ADD WIRE JUMPER W102 FROM U11F PIN 2 TO U6N PIN 3.
7. ADD WIRE JUMPER W103 FROM U7M PIN 1 TO U9J PIN 13.

		MATERIAL-	SIGNATURE	DATE	DIGI-DATA CORPORATION
		FINISH-	DR- D. HANSEL	10/30/80	8580 DORSEY RUN ROAD
		TOLERANCE-UNLESS	CHK- [illegible]	1-5-81	JESSUP, MD. 20794
		OTHERWISE SPECIFIED	ENG- [illegible]	1/5/81	SCALE: NONE SHEET 1 OF 1
		3 PLACE ± .005	CUST-		
		2 PLACE ± .010			ASSY, EMBEDDED FORMATTER
		FRACTIONS ± 1/64			
		ANGLES ± 1/2°			SIZE D DWG NO 0052645-0000 REV A
		DO NOT SCALE THIS PRINT			
BODY ASSY	USED ON				

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
01	CLASS 'B' RELEASE	6-17-18	JH

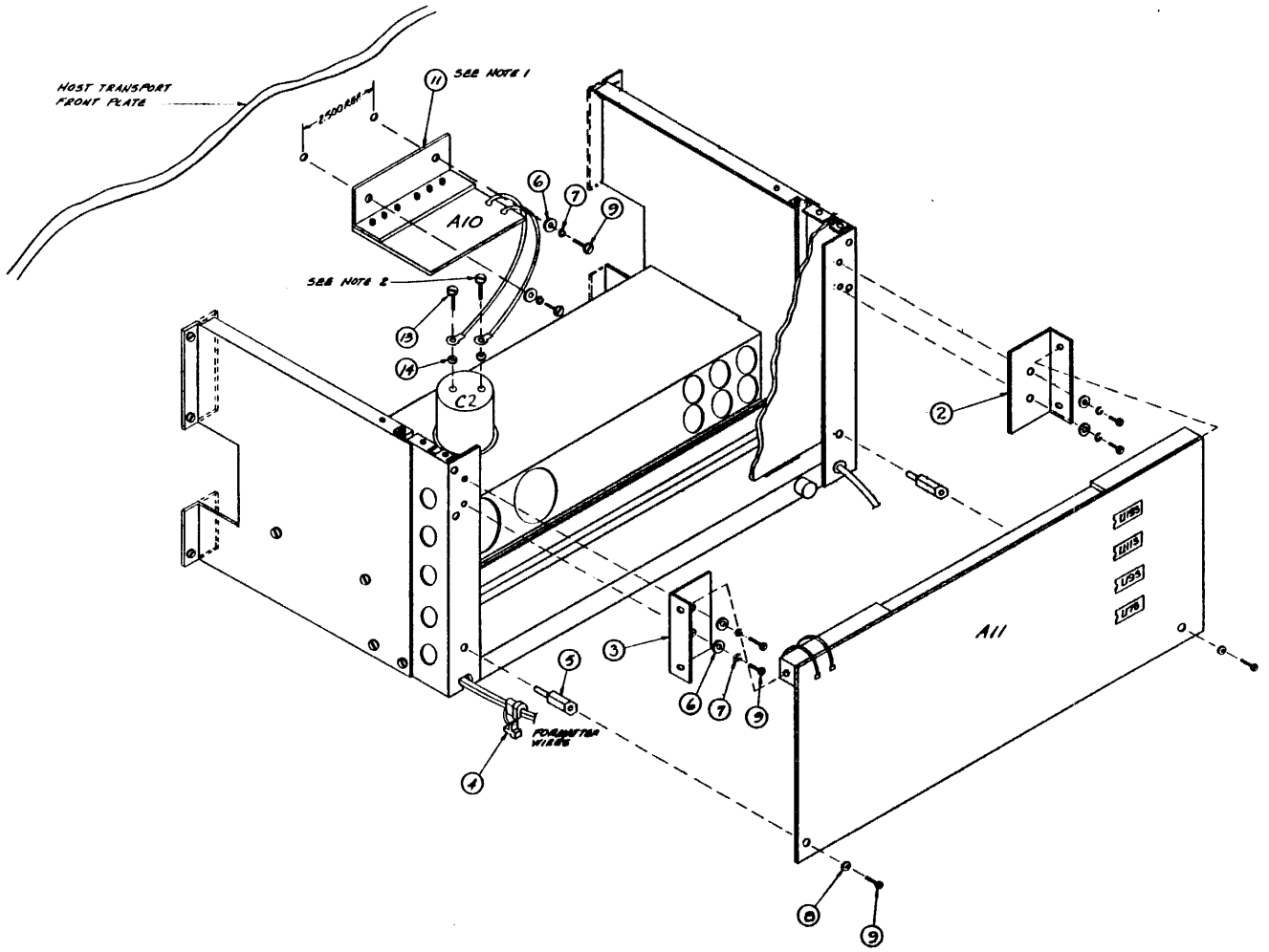


NOTES:

1. BOARD TO BE INDELIBLY STAMPED WITH ASSEMBLY NUMBER AND LATEST REV. LEVEL IN BLANK.
2. APPLY ITEM 34 TO BOTH SIDES OF ITEMS 32 & 33.

		MATERIAL-	SIGNATURE	DATE	DIGI-DATA CORPORATION 8580 DORSEY RUN ROAD JESSUP, MD. 20794
		FINISH-	DR- S. HEISTMAN	7/26/18	
		TOLERANCE-UNLESS OTHERWISE SPECIFIED 3 PLACE ± .005 2 PLACE ± .010 FRACTIONS ± 1/64 ANGLES ± 1/2°	CHK-		SCALE: 2:1 SHEET 1 OF 1
			ENG- JKEINA	6-17-18	
			CUST-		ASSEMBLY, FORMATTER POWER SUPPLY
0051533		DO NOT SCALE THIS PRINT			SIZE C DWG NO 0C 33-0000 REV 01
NEXT ASSY	USED ON				

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
01	CLASS "B" RELEASE	18 Mar 80	[illegible]



NOTES:

1. Apply item 13 between A10 mounting plate and host transport front plate.
2. After specified physical installation of kit has been made, make the following wire connections.
   A. Attach red wire from formatter power supply terminal, A10E4, to transport +8V filter capacitor, C2 (+). Replace existing screw with item 13 and use additional lockwasher item 14. Retain existing screw for step B.
   B. Attach black wire from formatter power supply ground terminal, A10E1, to transport +8V filter capacitor, C2 (-). Use screw from step A and use additional lockwasher item 14. Discard screw removed from C2(-) terminal.
   C. Attach orange +12V wire from transport connector J2-6 to formatter power supply +12V terminal E6.
   D. Attach green -12V wire from transport connector J1-N to formatter power supply -12V terminal E5.
   E. Attach black ground wire from embedded formatter ground terminal E8 to formatter power supply ground terminal E2.
   F. Attach red +5V wire from embedded formatter +5V terminal E4 to formatter power supply +5V terminal E3.
   G. Use item 12 to secure wires as required.
3. Some parts omitted for the sake of clarity.
4. Item 16, jumper terminals, to be shipped with each unit.

		MATERIAL-	SIGNATURE	DATE
		FINISH-	DR- S. KLASS	6-8-80
		TOLERANCE-UNLESS	CHK- T. CALC	1-5-81
		OTHERWISE SPECIFIED	ENG- [illegible]	1-5-81
		3 PLACE ± .005	CUST-	
		2 PLACE ± .010		
		FRACTIONS ± 1/64		
		ANGLES ± 1/2°		
NEXT ASSY	USED ON	DO NOT SCALE THIS PRINT		

DIGI-DATA CORPORATION
8580 DORSEY RUN ROAD
JESSUP, MD. 20794

SCALE: NONE | SHEET 1 OF 1

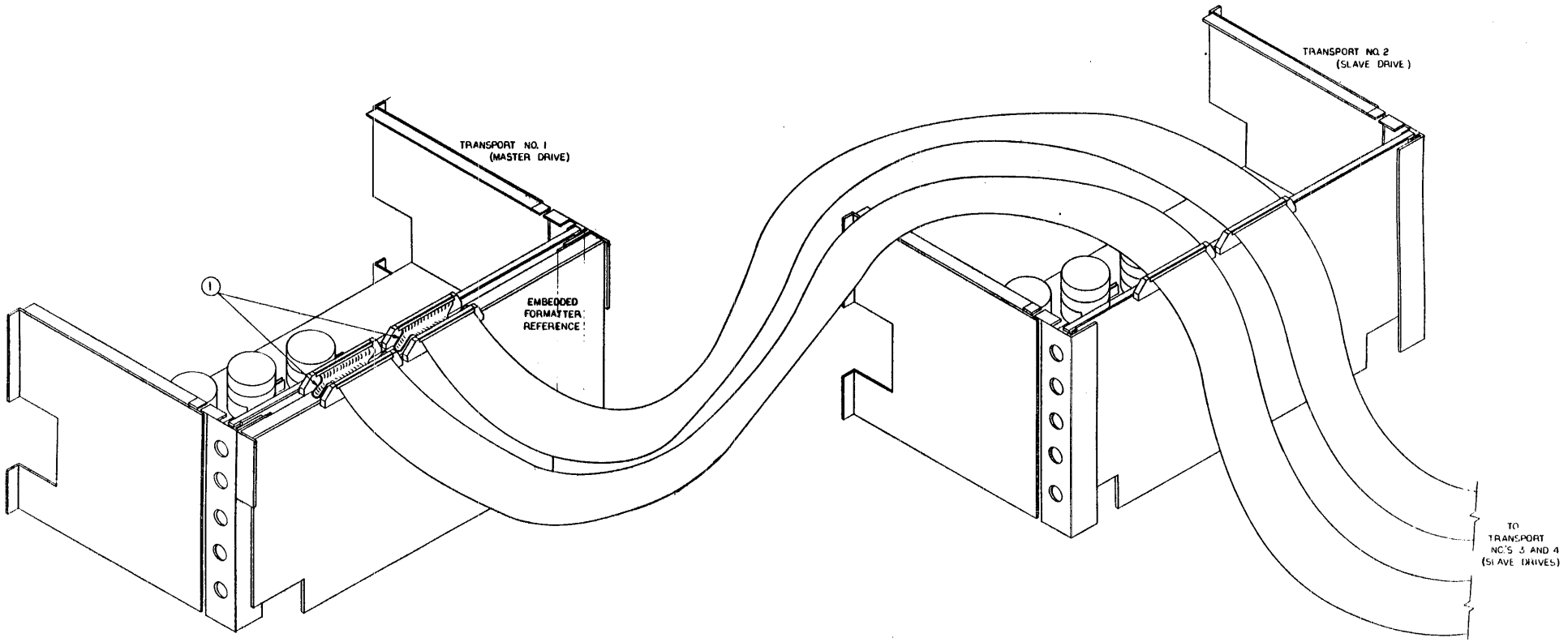
INSTALLATION DRAWING
FORMATTER KIT

SIZE D | DRG NO 0052701-0000 | REV 02

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
01	CLASS 'B' RELEASE	12-8-78	JH

NOTES:

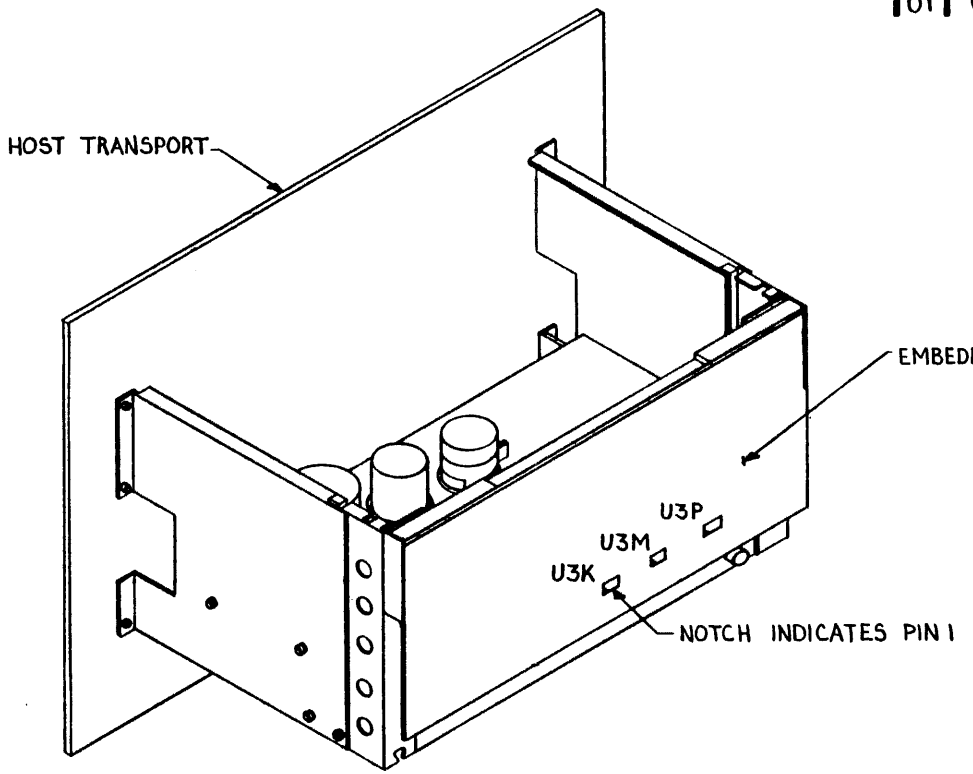
1. Some parts omitted for the sake of clarity.



		MATERIAL-	SIGNATURE	DATE	DIGI-DATA CORPORATION
		FINISH-	DR-S. HEISHMAN	11-30-79	8580 DORSEY RUN ROAD
		TOLERANCE-UNLESS	CHK-[illegible]	12-9-79	JESSUP, MD. 20794
		OTHERWISE SPECIFIED	ENG-	12-12-79	SCALE: NONE SHEET 1 OF 1
		3 PLACE ± .005	CUST-		
		2 PLACE ± .010			KIT; CABLE, EMBEDDED
		FRACTIONS ± 1/64			FORMATTER TO TRANSPORT
		ANGLES ± 1/2°			
		DO NOT SCALE THIS PRINT			SIZE D DWG NO 0052160-0000 REV 01
NEXT ASSY	USED ON				

AF 8603A

	REVISIONS		
LTR	DESCRIPTION	DATE	APPROVED
01	CLASS "B" RELEASE	12-30-80	PS / JPL



NOTES:
1. SOME PARTS OMITTED FOR THE SAKE OF CLARITY.

		MATERIAL-	SIGNATURE	DATE	DIGI-DATA CORPORATION 8580 DORSEY RUN ROAD JESSUP, MD. 20794
		FINISH-	DR- Kathy Bell	12-30-80	
		TOLERANCE-UNLESS	CHK- D. Speaker	12-30-80	
		OTHERWISE SPECIFIED	ENG- Mark Sanford	12-30-80	SCALE: NONE / SHEET 1 OF 1
		3 PLACE ± .005	CUST-		
		2 PLACE ± .010			KIT; FORMATTER TERMINATOR
		FRACTIONS ± 1/64			
		ANGLES ± 1/2°			
		DO NOT SCALE THIS			SIZE B / dwg no 0052702-0000 / REV 01
NEXT ASS'Y	USED ON	PRINT			

ITEM NO.	QTY.	PART NUMBER	DESCRIPTION	REFERENCE
1	1	1352296-0001	DRILL DETAIL 80 DEF	
2	1	2451122-9002	TTL GATE S SERIES	U7B
4	2	2451122-9004	TTL GATE S SERIES	U7C,U5M
5	9	2450053-9006	TTL GATE COMMERCIAL	SEE SHEET 4
6	1	2450053-9007	TTL GATE COMMERCIAL	U12L
7	1	2450052-9008	TTL GATE LS SERIES	U4N
10	1	2450052-9027	TTL GATE LS SERIES	U6M
11	1	2450052-9032	TTL GATE LS SERIES	U9H
12	3	2450064-9074	54/74 LS SERIES TTL D FLIP-FLOP	U13P,U13N,U6N
13	3	2452024-9074	TTL D FLIP-FLOP S SERIES	U5L,U10F,U9E
15	3	2451122-9086	TTL GATE S SERIES	U7M,U7D,U10C
17	3	2451339-9138	DECODERS/DEMULTIPLEXERS S SERIES	U13M,U7L,U11N
18	1	2451256-9151	DATA SELECTORS/MULTI LS SERIES	U7A
21	3	2451256-9155	DATA SELECTORS/MULTI LS SERIES	U11L,U12N,U5N
22	1	2452346-9157	DATA SELECTOR/MULTI, S SERIES	U8D
23	1	2451280-9169	SYN UP/DOWN COUNTERS LS SERIES	U8E
24	3	2451302-9173	REGISTERS LS SERIES	U8L,U12P,U11E
25	4	2451306-9174	FLIP-FLOPS, LS SERIES	U3H,U6L,U9M,U8M
27	1	2451331-9244	OCTAL BUFFERS LS SERIES	U10L
28	4	2451355-9251	DATA SELECTORS/MULTI S SERIES	U10N,U9N,U8N,U7N
29	2	2451310-9257	TRI-STATE DATA SELEC/MULTI LS SERIES	U4L,U5K
30	1	2452346-9258	DATA SELECTOR/MULTI, S SERIES	U6P
31	3	2451307-9259	ADDRESSABLE LATCH LS SERIES	U11M,U10M,U12M
32	2	2451301-9273	OCTAL LATCHES LS SERIES	U4S,U10H
34	4	2452347-9374	OCTAL LATCH, S SERIES	SEE SHEET 4
35	3	2451311-9395	CASCADABLE SHIFT REG LS SERIES	U8K,U9K,U10K
36	9	2451940-9837	HEX UNIFIED BUS RECEIVER	SEE SHEET 4
37	2	2150052-3101	TERMINATION PACK	U12J,U12F
38	1	2951474-0001	CRYSTAL OSCILLATOR	U9D
39	2	2451300-9001	MICROPROCESSOR	U9P,U11P
40	3	2452345-9911	MICROSEQUENCER	U5P,U5R,U5S

REV.	ECO NO.	DATE	APPR.
01	[illegible]	1/5/91	RS/JPL

REV.	ECO NO.	DATE	APPR.

DIGI-DATA CORPORATION

DR. [illegible] 1/4/91 ENG. [illegible] 1/5/91

CHK. [illegible] 1-5-91

TITLE
Assembly, Embedded Formatter
NRZ

SH. 1 | P.L. NO. 0052645-0001 | REV. A

0052645-0001

C1

D.D.C. FORM 105 REV. A

ITEM NO.	QTY.	PART NUMBER	DESCRIPTION	REFERENCE
41	1	2451386-0009	32x8 TRI-STATE PROM	U10E
42	1	2451386-0008	32x8 TRI-STATE PROM	U7P
46	1	2451361-0002	512x4 TRI-STATE PROM	U9L
50	1	2150004-0511	RES DEP CARBON,¼W,5% 510 OHM	R2A
53	12	2150004-0472	RES DEP CARBON,¼W,5%,4.7K OHM	SEE SHEET 4
54	1	2150004-0513	RES DEP CARBON,¼W,5%, 51K OHM	R1X
61	40	2250162-7104	CAP MONO CER,Z5U,100V,.1uF	SEE SHEET 4
64	1	2250166-7225	CAP SOLID TANT DIP,15V,2.2uF	C3N
65	4	2250166-7226	CAP SOLID TANT DIP,15V,22uF	C1C,C4D,C2N,C2X
70	2	2051226-0001	TERMINALS	EA,EB
72	6	2052256-0004	CONNECTOR STRAIGHT HEADERS	SEE SHEET 4
73	22	2951271-0001	STRAIGHT HEADER	SEE SHEET 4
74	1	1251451-0001	HINGE BAR	
75	3	5951539-0003	PRESS ON FASTENER	
76	3	2950006-0003	SOCKET, DIP, SOLDER TAIL	XU3K,XU3M,XU3P
77	4	2950006-0004	SOCKET, DIP, SOLDER TAIL	SEE SHEET 4
78	2	2950006-0005	SOCKET, DIP, SOLDER TAIL	XU9P,XU11P
79	AR	2050028-6000	WIRE, UL STYLE 1015	
80	AR	2050028-6222	WIRE, UL STYLE 1015	
81	2	2051128-4331	RECEPT, INSULATED, Q. D.	
82	2	2052339-0001	RECEPTACLE INSULATED FLAG	
83	REF	0052645-0000	ASSEMBLY; EMBEDDED FORMATTER PE/DUAL	
84	REF	0252341-0000	SCHEMATIC; FORMATTER	
85	AR	3950000-0001	SOLDER	
86	AR	2050025-0001	30 AWG INSULATED KYNAR WIRE	W101,W102

SH. 2 | P.L. NO. 0052645-0001 | REV. A

C2

D.D.C. FORM 117

ITEM	REFERENCE
5	U1S,U4M,U11D,U12D,U1H,U12K,U11K,U2H,U4R
34	U6R,U7R,U12R,U13R
36	U4K,U12H,U3J,U3L,U3N,U11F,U11J,U12E,U3R
53	R1S,R1J,R1H,R1K,R1R,R1T,R1V,R1W,R1Y,R1U,R2B,R1Z
61	C1H,C1S,C1Y,C2B,C2C,C2D,C2E,C2L,C2M,C2P,C2T,C2V,C2U,C2W,C2Y, C2Z,C3A,C3B,C3C,C3D,C3E,C3F,C3H,C3J,C3K,C3L,C3M,C3P,C3R,C3S, C3T,C3U,C3V,C3W,C3X,C3Y,C3Z,C4A,C4B,C4C
72	JA,JB,JC,JD,JE,JF
73	WA-WF,WH,WJ-WN,WP,WR,WS
77	XU7S,XU9S,XU11S,XU13S

size	dwg no	rev
A	0052645-0001	

SHEET 3 OF 3

C3

DDC Form 102

ITEM NO.	QTY.	PART NUMBER	DESCRIPTION	REFERENCE
1	1	1352296-0001	DRILL DETAIL 80 DEF	
2	1	2451122-9002	TTL GATE S SERIES	U7B
3	1	2450052-9004	TTL GATE LS SERIES	U8B
4	2	2451122-9004	TTL GATE S SERIES	U7C,U5M
5	9	2450053-9005	TTL GATE COMMERCIAL	SEE SHEET 4
6	2	2450053-9007	TTL GATE COMMERCIAL	U12L,U9A
7	1	2450052-9008	TTL GATE LS SERIES	U4N
8	1	2451122-9008	TTL GATE S SERIES	U2F
9	2	2450052-9011	TTL GATE LS SERIES	U4P,U7J
10	2	2450052-9027	TTL GATE LS SERIES	U9J,U6M
11	2	2450052-9032	TTL GATE LS SERIES	U7F,U9H
12	5	2450064-9074	54/74 LS SERIES TTL D FLIP-FLOP	SEE SHEET 4
13	5	2452024-9074	TTL D FLIP-FLOP S SERIES	SEE SHEET 4
14	1	2450052-9086	TTL GATE LS SERIES	U6K
15	3	2451122-9086	TTL GATE S SERIES	U7M,U7D,U10C
16	1	2450057-9124	TTL VOLT CONT OSC S SERIES	U10B
17	3	2451239-9138	DECODERS/DEMULTIPLEXERS S SERIES	U13M,U7L,U11N
18	1	2451256-9151	DATA SELECTORS/MULTI LS SERIES	U7A
19	1	2451338-9151	DATA SELECTORS/MULTI S SERIES	U9B
20	2	2451256-9153	DATA SELECTORS/MULTI LS SERIES	U1A,U3F
21	3	2451256-9155	DATA SELECTORS/MULTI LS SERIES	U11L,U12N,U5N
22	1	2452346-9157	DATA SELECTOR/MULTI, S SERIES	U8D
23	3	2451280-9169	SYN UP/DOWN COUNTERS LS SERIES	U8H,U8C,U8E
24	4	2451302-9173	REGISTERS LS SERIES	U8L,U12P,U8A,U11E
25	17	2451306-9174	FLIP-FLOPS, LS SERIES	SEE SHEET 4
26	16	2451492-9174	FLIP-FLOPS, S SERIES	SEE SHEET 4
27	1	2451331-9244	OCTAL BUFFERS LS SERIES	U10L
28	4	2451355-9251	DATA SELECTORS/MULTI S SERIES	U10N,U9N,U8N,U7N
29	2	2451310-9257	TRI-STATE DATA SELEC/MULTI LS SERIES	U4L,U5K
30	1	2452346-9258	DATA SELECTOR/MULTI, S SERIES	U6P
31	3	2451307-9259	ADDRESSABLE LATCH LS SERIES	U11M,U10M,U12M

DIGI-DATA CORPORATION

DR. [illegible] ENG. [illegible]

CHK. [illegible]

TITLE
Assembly, Embedded Formatter
PE, PE/NRZ

REV.	ECO NO.	DATE	APPR.	REV.	ECO NO.	DATE	APPR.
[illegible]							

SH.	P.L. NO.	REV.
1	0052645-0002	E

0052645-0002

D1

D.D.C. FORM 105 REV. A

ITEM NO.	QTY.	PART NUMBER	DESCRIPTION	REFERENCE
32	2	2451301-9273	OCTAL LATCHES LS SERIES	U4S,U10F
33	1	2451321-9280	PARITY GEN/CHECKER LS SERIES	U7H
34	4	2452347-9374	OCTAL LATCH, S SERIES	SEE SHEET 4
35	3	2451311-9395	CASCADABLE SHIFT REG LS SERIES	U8K,U9K,U10K
36	9	2451940-9037	HEX UNIFIED BUS RECEIVER	SEE SHEET 4
37	2	2150052-3101	TERMINATION PACK	U12J,U12F
38	1	2951474-0001	CRYSTAL OSCILLATOR	U9D
39	2	2451300-9001	MICROPROCESSOR	U9P,U11P
40	3	2452345-9911	MICROSEQUENCER	U5P,U6P,U8S
41	1	2451386-0009	32x8 TRI-STATE PROM	U10E
42	1	2451366-0008	32x8 TRI-STATE PROM	U7P
43	3	2451356-0002	256x4 TRI-STATE PROM	U6B,U3C,U6F
44	3	2451356-0003	256x4 TRI-STATE PROM	U5B,U2C,U5F
45	3	2451356-0004	256x4 TRI-STATE PROM	U4C,U1D,U4H
46	1	2451361-0002	512x4 TRI-STATE PROM	U9L
47	3	2451380-0002	256x8 TRI-STATE PROM	U6C,U3D,U6H
50	1	2150004-0511	RES DEP CARBON,¼W,5% 510 OHM	R2A
51	3	2150004-0102	RES DEP CARBON,¼W,5%,1K OHM	R1D,R1L,R1N
52	1	2150004-0222	RES DEP CARBON,¼W,5%,2.2K OHM	R1C
53	12	2150004-0472	RES DEP CARBON,¼W,5%,4.7K OHM	SEE SHEET 4
54	1	2150004-0513	RES DEP CARBON,¼W,5%, 51K OHM	R1X
55	1	2150020-1000	RES METAL FILM,1/8W,1%,100 OHM	R1F
56	1	2150020-1500	RES METAL FILM,1/8W,1%,150 OHM	R1E
57	1	2150020-6810	RES METAL FILM,1/8W,1%,681 OHM	R1A
58	1	2150020-7500	RES METAL FILM,1/8W,1%,750 OHM	R1B
59	1	2250163-3330	CAP MONO CER, COG,200V,33pF	C1J
60	1	2250163-3680	CAP MONO CER,COG,200V,68pF	C1U
61	57	2250162-7104	CAP MONO CER,Z5U,100V,.1uF	SEE SHEET 4
62	1	2250158-7105	CAP MONO CER,50V,1uF	C1N
63	1	2250166-7155	CAP SOLID TANT DIP,15V,1.5uF	C1M
64	2	2250166-7225	CAP SOLID TANT DIP,15V,2.2uF	C1P,C3N
65	5	2250166-7226	CAP SOLID TANT DIP,15V,22uF	SEE SHEET 4
66	2	2151636-0102	POTENTIOMETER, MULTITURN	R1M,R1P
67	3	2550002-9140	DIODE SILICON FAST SWITCHING	CR1A,CR1B,CR1C
68	1	2350017-0001	TRANSISTOR, PNP, SILICON	QA
69	1	2951520-0001	CHOKE	LA
70	2	2051226-0001	TERMINALS	EA,EB
72	6	2052256-0004	CONNECTOR STRAIGHT HEADERS	SEE SHEET 4

SH.	P.L. NO.	REV.
2	0052645-0002	A

D2

D.D.C. FORM 117

ITEM NO.	QTY.	PART NUMBER	DESCRIPTION	REFERENCE
73	22	2951271-0001	STRAIGHT HEADER	SEE SHEET 4
74	1	1251451-0001	HINGE BAR	
75	3	5951539-0003	PRESS ON FASTENER	
76	3	2950006-0003	SOCKET, DIP, SOLDER TAIL	XU3K,XU3M,XU3P
77	4	2950006-0004	SOCKET, DIP, SOLDER TAIL	SEE SHEET 4
78	2	2950006-0005	SOCKET, DIP, SOLDER TAIL	XU9P,XU11P
79	AR	2050028-6000	WIRE, UL STYLE 1015	
80	AR	2050028-6222	WIRE, UL STYLE 1015	
81	2	2051128-4331	RECEPT, INSULATED, Q. D.	
82	2	2052339-0001	RECEPTACLE INSULATED FLAG	
83	REF	0052645-0000	ASSEMBLY; EMBEDDED FORMATTER PE/DUAL	
84	REF	0252341-0000	SCHEMATIC; FORMATTER	
85	AR	3950000-0001	SOLDER	
86	AR	2050025-0001	30 AWG INSULATED KYNAR WIRE	W101,W102,W103

SH.	P.L. NO.	REV.
3	0052645-0002	A

D3

D.D.C. FORM 117

ITEM	REFERENCE
5	U1S,U4M,U11D,U12D,U1H,U12K,U11K,U2H,U4R
12	U13P,U13N,U11H,U6N,U10D
13	U5L,U8F,U9F,U10F,U9E
25	U5A,U4B,U7E,U5D,U1F,U1C,U2E,U2B,U3H,U4F,U5J,U8J,U5E,U6L,U9M, U8M,U7K
26	U5C,U6D,U6A,U4D,U2D,U3B,U1E,U3E,U5H,U6J,U6E,U4J,U9C,U4E,U1B, U4A
34	U6R,U7R,U12R,U13R
36	U4K,U12H,U3J,U3L,U3N,U11F,U11J,U12E,U3R
53	R1S,R1J,R1H,R1K,R1R,R1T,R1V,R1W,R1Y,R1U,R2B,R1Z
61	C1A,C1D,C1E,C1F,C1H,C1L,C1W,C1X,C1R,C1S,C1T,C1Y,C1Z,C2A,C2B, C2C,C2D,C2E,C2F,C2H,C2J,C2K,C2L,C2M,C2P,C2R,C2S,C2T,C2V,C2U, C2W,C2Y,C2Z,C3A,C3B,C3C,C3D,C3E,C3F,C3H,C3J,C3K,C3L,C3M,C3P, C3R,C3S,C3T,C3U,C3V,C3W,C3X,C3Y,C3Z,C4A,C4B,C4C
65	C1C,C4D,C1B,C2N,C2X
72	JA,JB,JC,JD,JE,JF
73	WA-WF,WH,WJ-WN,WP,WR,WS
77	XU7S,XU9S,XU11S,XU13S

size	dwg no	rev
A	0052645-0002	01

SHEET 4 OF 4

D4

DDC Form 102

ITEM	QTY/DASH 1	PART NUMBER	DESCRIPTION	REFERENCE
1	1	1351534-0001	DRILL DETAIL, 78 FPS ,	
2	1	2450050-3611	QUAD OP AMP	U1
3	5	2350025-3055	TRANSISTOR, SIL., 90W, NPN	Q1,Q2,Q3,Q4,Q5
4	1	2350022-6400	SI. CONT. RECTIFIER, 16A	Q6
5	1	2350023-0010	TRANSISTOR, 1W, NPN	Q7
6	1	2350017-0001	TRANSISTOR, PNP SILICON	Q8
7	1	2550009-2569	DIODE, ZENER, 1W,5.6V, 5%	CR4
8	3	2550002-9140	DIODE, SIL., FAST SWITCHING	CR1,CR2,CR3
9	1	2150004-0120	RESISTOR, D.C., 1/4W, 5%, 12 Ohm	R29
10	2	2150004-0101	RESISTOR, D.C., 1/4W, 5%, 100 Ohm	R16,R30
11	5	2150004-0102	RESISTOR, D.C., 1/4W,5%, 1K Ohm	R6,R7,R14,R17
				R23
12	1	2150004-0153	RESISTOR,D.C.,1/4W,5%, 15K Ohm	R26
13	1	2150004-0243	RESISTOR,D.C.,1/4W,5%, 24K Ohm	R27
14	1	2150004-0103	RESISTOR,D.C.,1/4W,5%,100K Ohm	R18
15	1	2150038-0180	RESISTOR,W.W.,2W,5%,18 Ohm	R25
16	5	2150037-0108	RESISTOR,W.W.,2W,5%,0.1 Ohm	R9,R10,R11,R12,
				R13
17	1	2150046-1203	POTENTIOMETER,20K Ohm	R28

BASIC / VERSION

NOTES:

P.L. NO. 0051533-0001

REV.	CHG. NO.	DATE	APPR.	NEXT ASSY.	USED ON
-	-	7-31-78	JPK	0051544-0003	
02	ECO-447	1-16-80	JK	0051544-0002	
01	CL 'B' REL	8-17-78	JPK	0051544-0001	

DIGI-DATA CORPORATION

DR RJB 7-5-78 ENG JPK 7-17-78

CHK

TITLE: ASSEMBLY; FORMATTER POWER SUPPLY

P.L. NO. 0051533-0001 SH. 1 OF 3 REV. 03

E1

D.D. FORM 04-1-50001-0000

ITEM	QTY/DASH 1	PART NUMBER	DESCRIPTION	REFERENCE
			CAPACITORS, MONOLITHIC CERAMIC	
18	4	2250162-7103	100V,-20,+80%,Z5U,.01uF	C2,C6,C7,C10
19	2	2250161-4183	100V,10%,X7R,.018uF	C3,C4
20	2	2250162-7104	100V,-20,+80%,Z5U,0.1uF	C9,C12
21	4	2250166-5226	CAPACITOR, DIPPED TANTALUM, 20%,15V,22uF	C1,C5,C8,C11
22	1	2150020-1001	RESISTOR,METAL FILM,1/8W,1.00K Ohm	R21
23	1	2150020-1471	RESISTOR,METAL FILM,1/8W,1.47K Ohm	R22
24	5	2150020-4991	RESISTOR,METAL FILM,1/8W,4.99K Ohm	R1,R2,R3,R4,R5
25	2	2150020-1002	RESISTOR,METAL FILM,1/8W,10.0K Ohm	R8,R19
26	1	2150020-1052	RESISTOR,METAL FILM,1/8W,10.5K Ohm	R24
27	2	2150020-2612	RESISTOR,METAL FILM,1/8W,26.1K Ohm	R15,R20
28	1	1151532-0001	HEAT SINK BRACKET	
29	1	2060001-0004	FUSE,AGC,10A	F1
30	2	2950019-0001	FUSE CLIP, P.C.	
31	6	2051226-0001	TERMINALS	E1,E2,E3,E4,E5,
				E6
32	5	2950011-0001	INSULATOR, MICA	
33	1	2950010-0001	INSULATOR, MICA	
34	AR	9050001-0001	SILICONE HEAT SINK COMPOUND	
35	6	5050021-0206	SCR.,BDR.HD., 4-40 x 3/8. S.S.	
36	6	5250005-1202	WSHR.,LK.,INT. TH., #4	

BASIC / VERSION

NOTES:

P.L. NO. 0051533-0001

DIGI-DATA CORPORATION

DR ENG

CHK

TITLE: ASSEMBLY; FORMATTER POWER SUPPLY

P.L. NO. 0051533-0001 SH. 2 OF 3 REV. 01

E2

D.D. FORM 04-1-50001-0000

ITEM	QTY/DASH 1	PART NUMBER	DESCRIPTION	REFERENCE
37	6	5150001-1203	NUT, HEX, 4-40	
38	REF	0251536-0000	SCHEMATIC, FORMATTER POWER SUPPLY	
39	REF	0051533-0000	ASSEMBLY; FORMATTER POWER SUPPLY	
40	2	2051128-4331	RECEPTACLE, INSULATED, QUICK DISCONNECT, .250, BLUE	
41	2	2051119-0017	TERMINAL, INSULATED RING, #10, BLUE	
42	AR	2050028-6000	WIRE, UL 1015, 14 AWG, BLACK	
43	AR	2050028-6777	WIRE, UL 1015, 14 AWG, VIOLET	

BASIC / VERSION

NOTES:

P.L. NO. 0051533-0001

DIGI-DATA CORPORATION

DR ENG

CHK

TITLE: ASSEMBLY; FORMATTER POWER SUPPLY

P.L. NO. 0051533-0001 SH. 3 OF 3 REV.

E3

D.D. FORM 04-1-50001-0000

ITEM NO.	QTY.	PART NUMBER	DESCRIPTION	REFERENCE
1	1	0052645-0001	ASSEMBLY; FORMATTER NRZ	A11
2	1	1152697-0001	FORMATTER BRACKET	
3	1	1152697-0002	FORMATTER BRACKET	
4	1	5950000-0001	STRAIN RELIEF	
5	2	5350002-0003	SPACER, HEX	
6	6	5250008-1206	WASHER, FLAT, #6	
7	6	5250004-1205	WASHER, LOCK, #6	
8	2	5250007-1104	WASHER, FLAT, NYLON #6	
9	8	5050005-0305	SCREW, BDR. HD., #6-32 x 5/16 LG.	
10	1	0051533-0001	ASSEMBLY; FORMATTER POWER SUPPLY	A10
11	AR	9050001-0001	SILICONE HEAT SINK COMPOUND	
12	AR	5951759-0001	CABLE TIE	
13	1	5050005-0608	SCREW, BDR HD, 10-32 x ½ LG	
14	2	5250005-1205	WASHER, LOCK, INT. TOOTH, #10	
15	REF	0052701-0000	INSTALLATION DWG.; FORMATTER KIT	
16	7	2051274-0001	JUMPER TERMINAL	
17				
18	1	2452506-0023	512 x 8 TRI-STATE PROM	A11,U11S
19	1	2452506-0024	512 x 8 TRI-STATE PROM	A11,U7S
20	1	2452506-0022	512 x 8 TRI-STATE PROM	A11,U13S
21	1	2452506-0025	512 x 8 TRI-STATE PROM	A11,U9S

DIGI-DATA CORPORATION

DR. | ENG. | CHK.

TITLE
Embedded Formatter Kit, NRZ

REV.	ECO NO.	DATE	APPR.	REV.	ECO NO.	DATE	APPR.	SH.	P.L. NO.	REV.
								1	0052701-0001	01

D.D.C. FORM 105 REV. A

0052701-0001

A1

ITEM #	QTY	PART NO.	DESCRIPTION	REFERENCE
1	1	0052645-0002	ASSEMBLY; FORMATTER PE, PE/NRZ	A11
2	1	1152697-0001	FORMATTER BRACKET	
3	1	1152697-0002	FORMATTER BRACKET	
4	1	5950000-0001	STRAIN RELIEF	
5	2	5350002-0003	SPACER, HEX	
6	6	5250008-1206	WASHER, FLAT, #6	
7	6	5250004-1205	WASHER, LOCK, #6	
8	2	5250007-1104	WASHER, FLAT, NYLON #6	
9	8	5050005-0305	SCREW, BDR. HD., #6-32 x 5/16 LG.	
10	1	0051533-0001	ASSEMBLY; FORMATTER POWER SUPPLY	A10
11	AR	9050001-0001	SILICONE HEAT SINK COMPOUND	
12	AR	5951759-0001	CABLE TIE	
13	1	5050005-0608	SCREW, BDR HD, 10-32 x ½ LG	
14	2	5250005-1205	WASHER, LOCK, INT. TOOTH, #10	
15	REF	0052701-0000	INSTALLATION DWG.; FORMATTER KIT	
16	7	2051274-0001	JUMPER TERMINAL	
17				
18	1	2452506-0044	512 x 8 TRI-STATE PROM	A11,U11S
19	1	2452506-0045	512 x 8 TRI-STATE PROM	A11,U7S
20	1	2452506-0043	512 x 8 TRI-STATE PROM	A11,U13S
21	1	2452506-0046	512 x 8 TRI-STATE PROM	A11,U9S

TITLE: EMBEDDED FORMATTER KIT, PE | SCALE REF: | PART NO. 0052701-0002 | REV: 02

DIGI-DATA CORPORATION | UNLESS OTHERWISE SPECIFIED XX: ±.010 XXX: ±.005 ANGLES: ± ½° | DO NOT SCALE THIS DRAWING | SHT: 1

DDC FORM 120

ITEM #	QTY	PART NO.	DESCRIPTION	REFERENCE
1	1	0052645-0002	ASSEMBLY; FORMATTER PE, PE/NRZ	A11
2	1	1152697-0001	FORMATTER BRACKET	
3	1	1152697-0002	FORMATTER BRACKET	
4	1	5950000-0001	STRAIN RELIEF	
5	2	5350002-0003	SPACER, HEX	
6	6	5250008-1206	WASHER, FLAT, #6	
7	6	5250004-1205	WASHER, LOCK, #6	
8	2	5250007-1104	WASHER, FLAT, NYLON #6	
9	8	5050005-0305	SCREW, BDR. HD., #6-32 x 5/16 LG.	
10	1	0051533-0001	ASSEMBLY; FORMATTER POWER SUPPLY	A10
11	AR	9050001-0001	SILICONE HEAT SINK COMPOUND	
12	AR	5951759-0001	CABLE TIE	
13	1	5050005-0608	SCREW, BDR HD, 10-32 x ½ LG	
14	2	5250005-1205	WASHER, LOCK, INT. TOOTH, #10	
15	REF	0052701-0000	INSTALLATION DWG.; FORMATTER KIT	
16	7	2051274-0001	JUMPER TERMINAL	
17				
18	1	2452506-0048	1024 x 8 TRI-STATE PROM	A11,U11S
19	1	2452506-0049	1024 x 8 TRI-STATE PROM	A11,U7S
20	1	2452506-0047	1024 x 8 TRI-STATE PROM	A11,U13S
21	1	2452506-0050	1024 x 8 TRI-STATE PROM	A11,U9S

TITLE: EMBEDDED FORMATTER KIT, PE/NRZ | SCALE REF | PART NO 0052701-0003 | REV:

DIGI-DATA CORPORATION | UNLESS OTHERWISE SPECIFIED XX: ±.010 XXX: ±.005 ANGLES: ± ½° | DO NOT SCALE THIS DRAWING | SHT: 1

ITEM NO.	QTY.	PART NUMBER	DESCRIPTION	REFERENCE
1	2	2051579-0001	CABLE	
2	REF	0052160-0000	KIT; CABLE, EMBEDDED FORMATTER TO TRANSPORTS	

DIGI-DATA CORPORATION

DR. [illegible] ENG. [illegible] 12-12-79

CHK. WBF 12-7-79

TITLE KIT; CABLE, EMBEDDED FORMATTER TO ONE TRANSPORT

REV.	CHG. NO.	DATE	APPR.	NEXT ASSY.	P.L. NO.	SH.	OF	REV.
01	CL. 3 REL.	12-12-79	JJK		0052160-0001	1	1	01

0052160-0001

B1

ITEM NO.	QTY.	PART NUMBER	DESCRIPTION	REFERENCE
1	2	2051579-0002	CABLE	
2	REF	0052160-0000	KIT; CABLE, EMBEDDED FORMATTER TO TRANSPORTS	

DIGI-DATA CORPORATION

DR. [illegible] 12-12-79 ENG. JJK 12-12-79

CHK. WBF 12-7-79

TITLE KIT; CABLE, EMBEDDED FORMATTER TO TWO TRANSPORTS

REV.	CHG. NO.	DATE	APPR.	NEXT ASSY.	P.L. NO.	SH.	OF	REV.
01	CL. 3 REL.	12-12-79	JJK		0052160-0002	1	1	01

0052160-0002

B2

ITEM NO.	QTY.	PART NUMBER	DESCRIPTION	REFERENCE
1	2	2051579-0003	CABLE	
2	REF	0052160-0000	KIT; CABLE, EMBEDDED FORMATTER TO TRANSPORTS	

DIGI-DATA CORPORATION

DR. [illegible] ENG. [illegible]

CHK. [illegible] 12-7-79

TITLE KIT; CABLE, EMBEDDED FORMATTER TO THREE TRANSPORTS

REV.	CHG. NO.	DATE	APPR.	NEXT ASSY.	P.L. NO.	SH.	OF	REV.
		[illegible]			0052160-0003	1	1	

0052160-0003

B-3

ITEM NO.	QTY.	PART NUMBER	DESCRIPTION	REFERENCE
1	2	2051579-0004	CABLE	
2	REF	0052160-0000	KIT; CABLE, EMBEDDED FORMATTER TO TRANSPORTS	

DIGI-DATA CORPORATION

DR. [illegible] ENG. [illegible] 12-12-79

CHK. [illegible] 12-7-79

TITLE KIT; CABLE, EMBEDDED FORMATTER TO FOUR TRANSPORTS

REV.	CHG. NO.	DATE	APPR.	NEXT ASSY.	P.L. NO.	SH.	OF	REV.
		[illegible]			0052160-0004	1	1	

0052160-0004

B4

ITEM NO.	QTY.	PART NUMBER	DESCRIPTION	REFERENCE
1	3	2150052-3101	RESISTOR TERMINATOR PACK	U3K,U3M,U3P
2	REF	0052702-0000	KIT FORMATTER TERMINATOR	

REV.	ECO NO.	DATE	APPR.	REV.	ECO NO.	DATE	APPR.
01	CLASS "B" REL	1/5/81	RS/JK				

DIGI-DATA CORPORATION

DR. RS	1/5/81	ENG. P.S.	1/5/81
CHK. JK	1-5-81		

TITLE
KIT FORMATTER, TERMINATOR

SH.	P.L. NO.	REV.
1	0052702-0001	01

D.D.C. FORM 105 REV. A